Chapter 4
Field-Effect Transistors

Microelectronic Circuit Design

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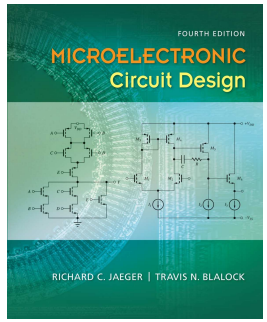
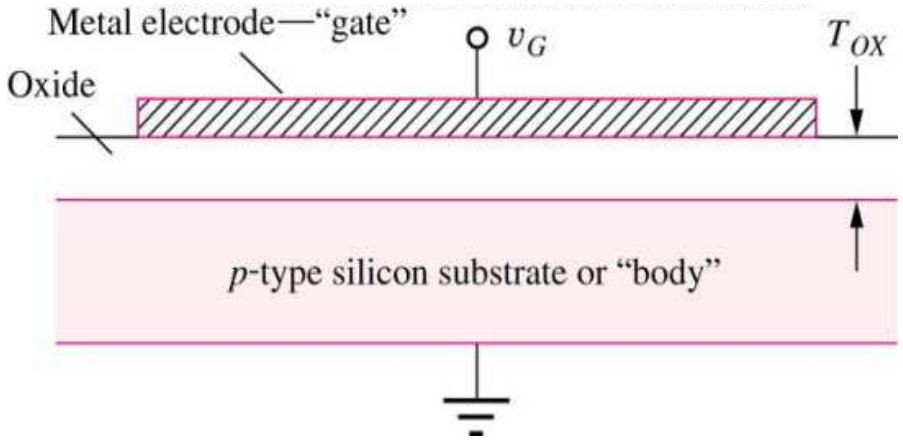


Chapter Goals

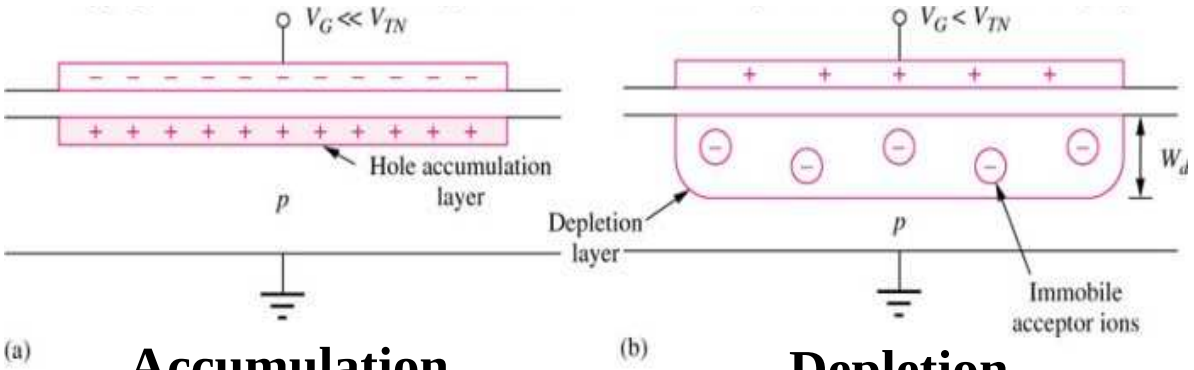
- Describe operation of MOSFETs.
- Define FET characteristics in operation regions of cutoff, triode and saturation.
- Develop mathematical models for *i*-*v* characteristics of MOSFETs.
- Introduce graphical representations for output and transfer characteristic descriptions of electron devices.
- Define and contrast characteristics of enhancement-mode and depletion-mode FETs.
- Define symbols to represent FETs in circuit schematics.
- Investigate circuits that bias transistors into different operating regions.
- Learn basic structure and mask layout for MOS transistors and circuits.
- Explore MOS device scaling
- Contrast 3 and 4 terminal device behavior.
- Describe sources of capacitance in MOSFETs.
- Explore FET modeling in SPICE.

MOS Capacitor Structure

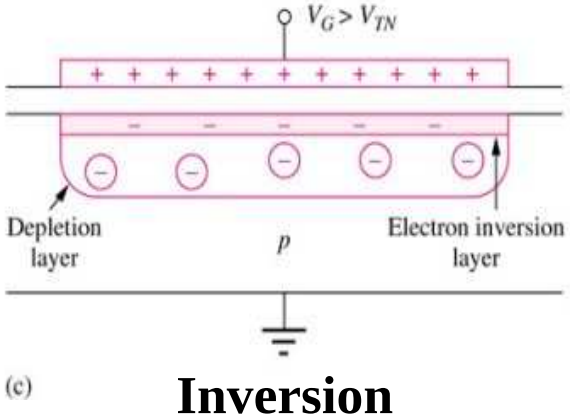


- First electrode - Gate: Consists of low-resistivity material such as metal or doped polycrystalline silicon
- Second electrode - Substrate or Body: *n*- or *p*-type semiconductor
- Dielectric - Silicon dioxide: stable high-quality electrical insulator between gate and substrate.

Substrate Conditions for Different Biases



Accumulation **Depletion**



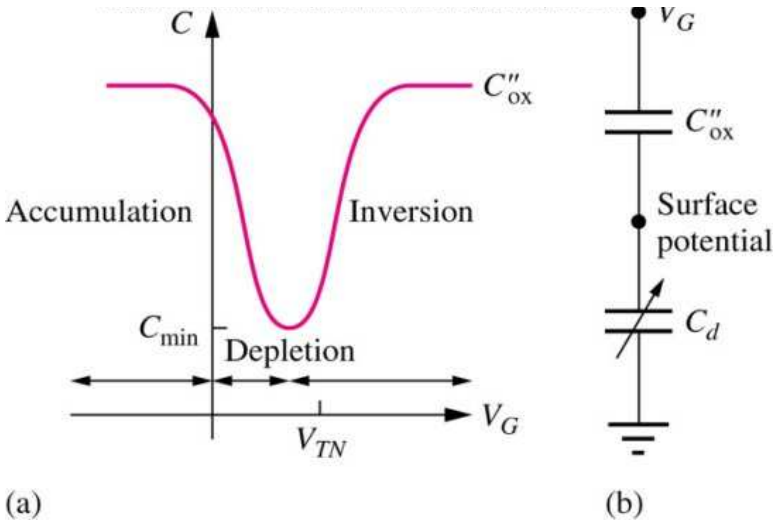
Inversion

Accumulation
- $V_G << V_{TN}$

Depletion
- $V_G < V_{TN}$

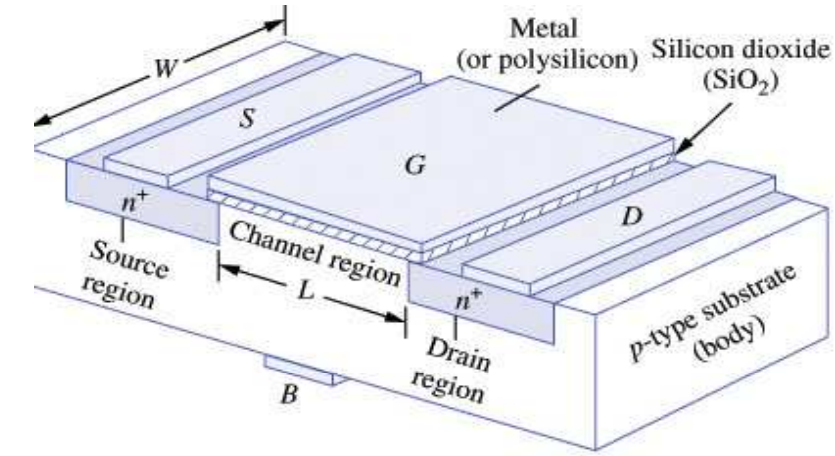
Inversion
- $V_G > V_{TN}$

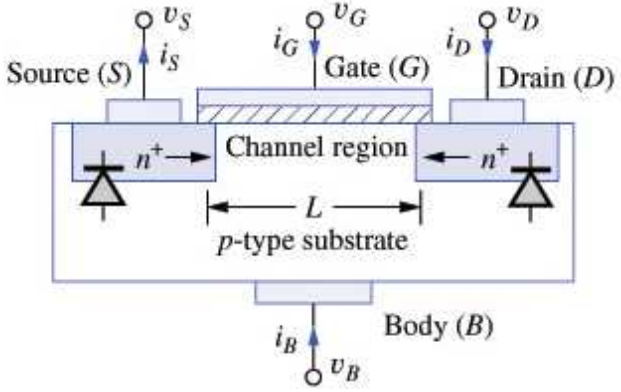
Low-frequency C-V Characteristics for an MOS Capacitor on p-type Substrate

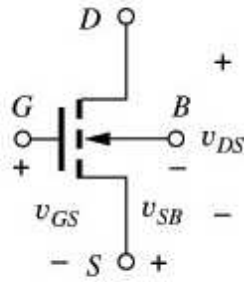


- MOS capacitance is a non-linear function of voltage.
- Total capacitance in any region is dictated by the separation between capacitor plates.
- Total capacitance modeled as series combination of fixed oxide capacitance and voltage-dependent depletion-layer capacitance.

NMOS Transistor:
Structure

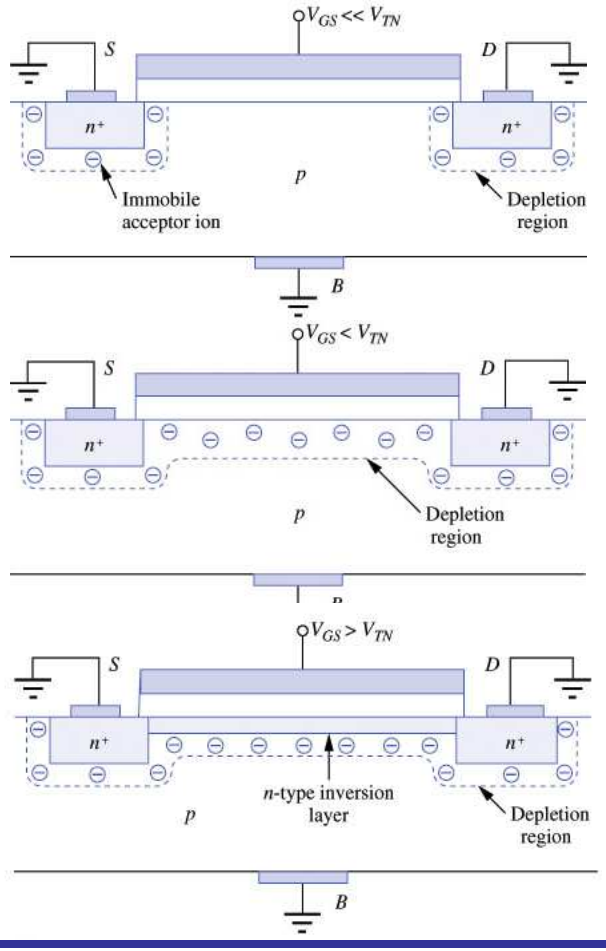






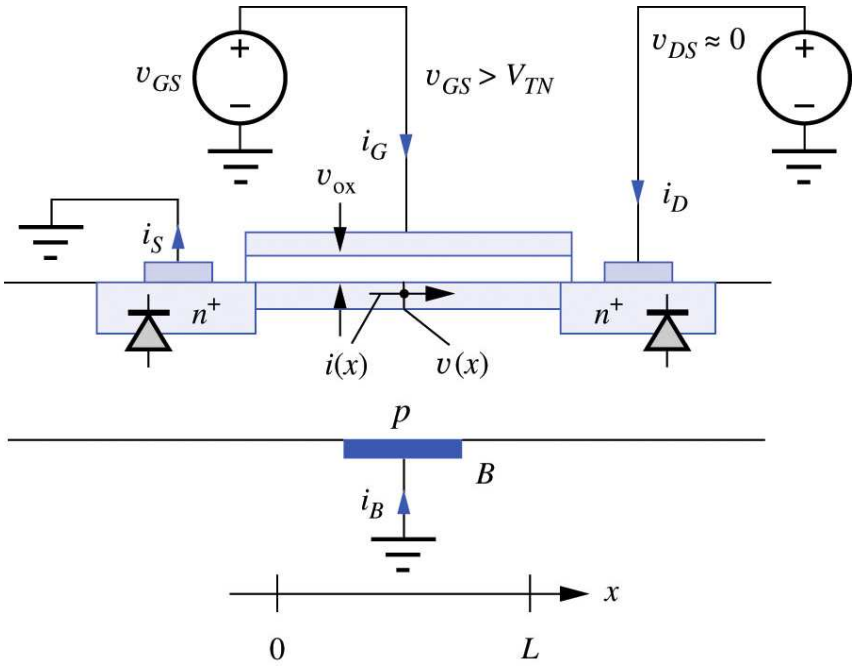
- 4 device terminals: Gate(G), Drain(D), Source(S) and Body(B).
- Source and drain regions form *pn* junctions with substrate.
- v_{SB}, v_{DS} and v_{GS} always positive during normal operation.
- v_{SB} always < v_{DS} and v_{GS} to reverse bias *pn* junctions

NMOS Transistor:
Qualitative I-V Behavior



- $V_{GS} << V_{TN}$: Only small leakage current flows.
- $V_{GS} < V_{TN}$: Depletion region formed under gate merges with source and drain depletion regions. No current flows between source and drain.
- $V_{GS} > V_{TN}$: Channel formed between source and drain. If $v_{DS} > 0$, finite i_D flows from drain to source.
- $i_B = 0$ and $i_G = 0$.

NMOS Transistor:
Triode Region Characteristics



$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}$$

for $v_{GS} - V_{TN} \geq v_{DS} \geq 0$

$$K_n = K_n' W/L$$

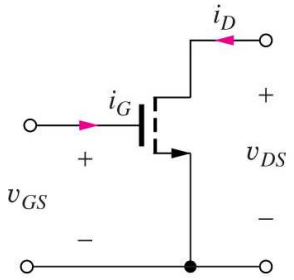
$$K_n' = \mu_n C_{ox}'' \quad (\text{A/V}^2)$$

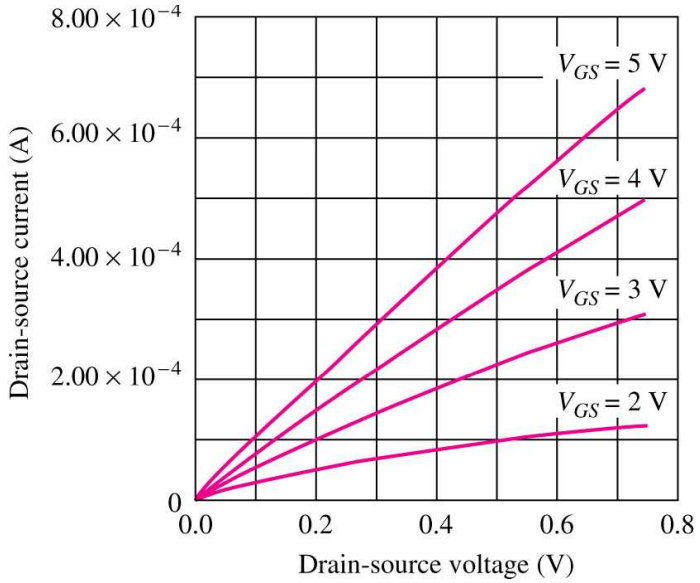
$$C_{ox}'' = \varepsilon_{ox}/T_{ox}$$

ε_{ox} = oxide permittivity (F/cm)

T_{ox} = oxide thickness (cm)

NMOS Transistor:
Triode Region Characteristics (cont.)

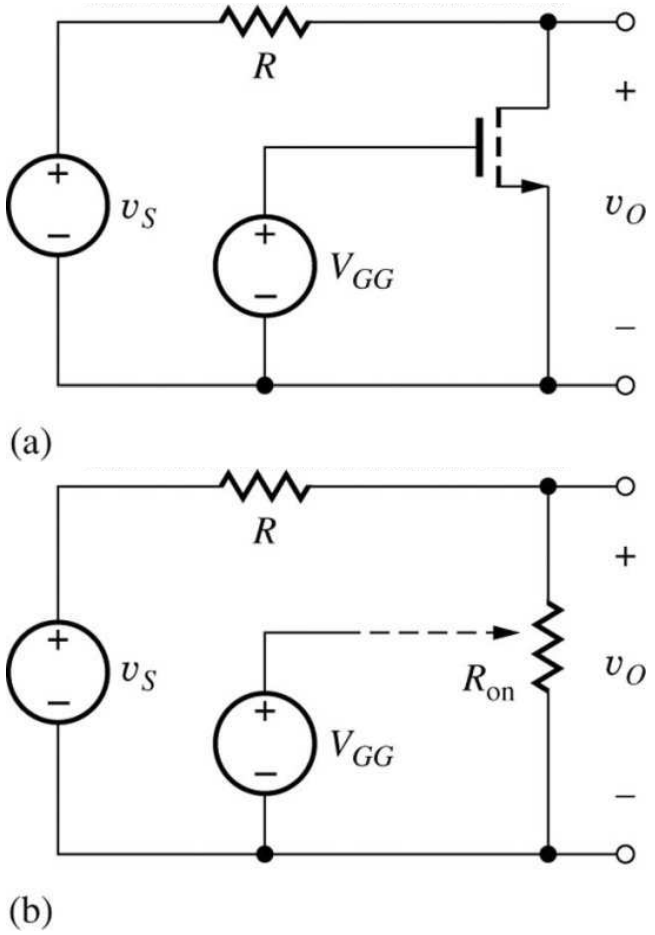




- Output characteristics appear to be linear.
- FET behaves like a gate-source voltage-controlled resistor between source and drain with

$$R_{on} = \left[\left. \frac{\partial i_D}{\partial v_{DS}} \right|_{v_{DS} \to 0} \right]^{-1}_{Q-Pt} = \left. \frac{1}{K_n' \frac{W}{L} \left(V_{GS} - V_{TN} - V_{DS} \right)} \right|_{V_{DS} \to 0} = \frac{1}{K_n' \frac{W}{L} \left(V_{GS} - V_{TN} \right)}$$

MOSFET as a Voltage-Controlled Resistor



Example 1: Voltage-Controlled Attenuator

$$\frac{v_O}{v_S} = \frac{R_{on}}{R_{on} + R} = \frac{1}{1 + K_n R\left(V_{GG} - V_{TN}\right)}$$

If $K_n = 500\mu A/V^2$, $V_{TN} = 1V$, $R = 2k\Omega$ and $V_{GG} = 1.5V$, then,

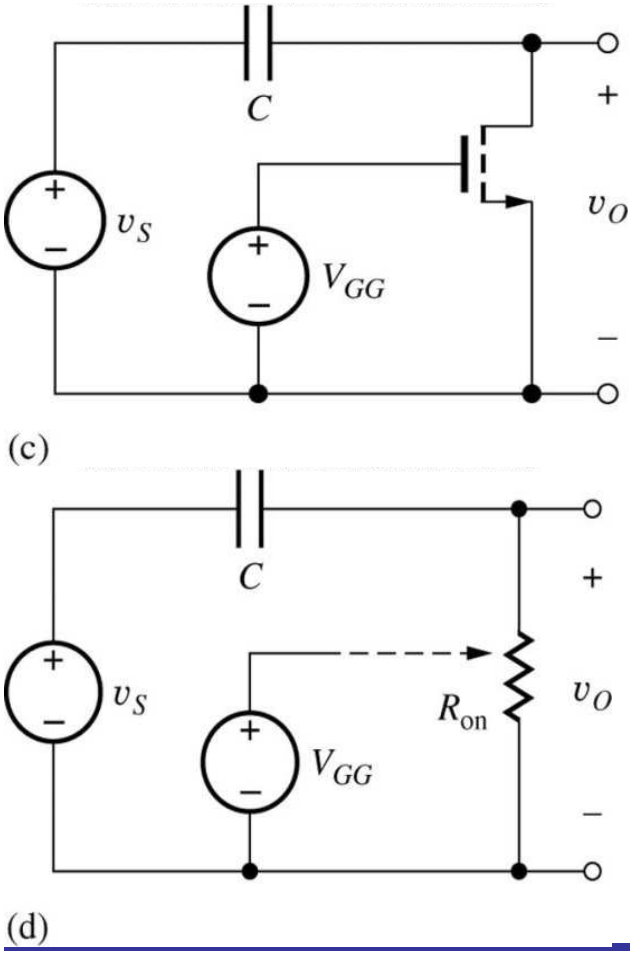
$$\frac{v_O}{v_S} = \frac{1}{1 + 500\frac{\mu A}{V^2}(2000\Omega)(1.5 - 1)V} = 0.667$$

To maintain triode region operation,

$$v_{DS} \le v_{GS} - V_{TN} \quad \text{or} \quad v_O \le V_{GG} - V_{TN}$$

$$0.667 v_S \le (1.5 - 1)V \quad \text{or} \quad v_S \le 0.750\ V$$

MOSFET as a Voltage-Controlled Resistor (cont.)



Example 2: Voltage-Controlled High-Pass Filter

Voltage Transfer function, $T(s) = \frac{V_O(s)}{V_S(s)} = \frac{s}{s+\omega_o}$

where, cut-off frequency

$$\omega_o = \frac{1}{R_{on}C} = \frac{K_n(V_{GS} - V_{TN})}{C}$$

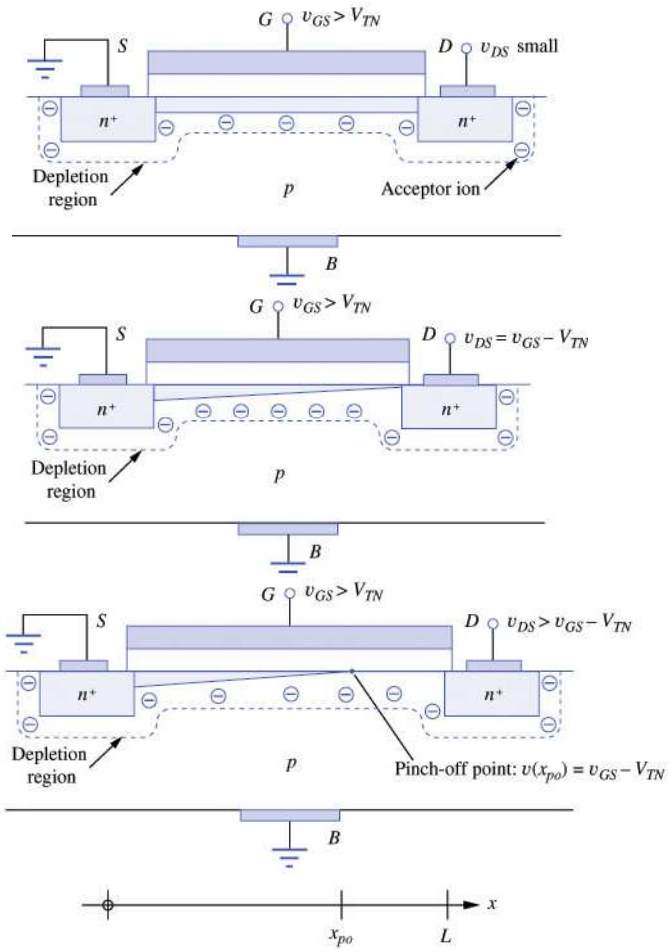
If $K_n = 500\mu A/V^2$, $V_{TN} = 1V$, $C = 0.02\mu F$ and $V_{GG} = 1.5V$, then,

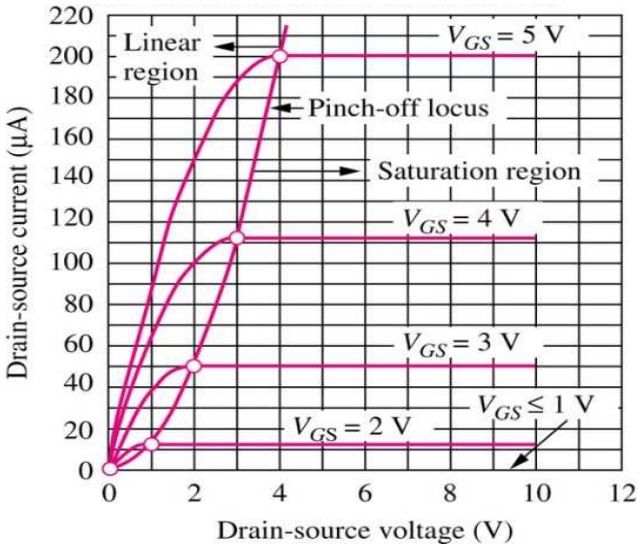
$$f_o = \frac{500\frac{\mu A}{V^2}(1.5-1)V}{2\pi(0.02\mu F)} = 1.99\ kHz$$

To maintain triode region operation,

$$v_S \le V_{GG} - V_{TN} = 0.5\ V$$

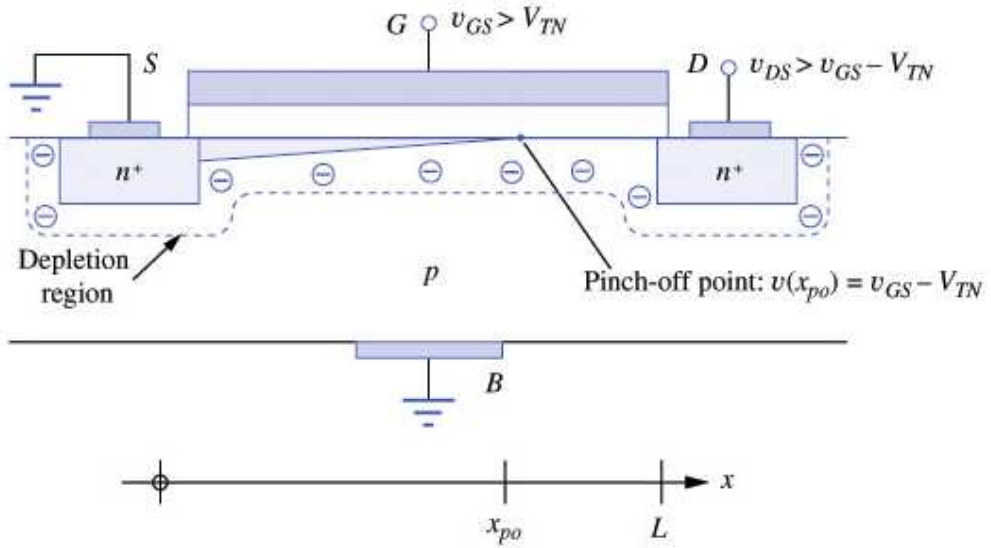
NMOS Transistor:
Saturation Region





- If v_{DS} increases above triode region limit, the channel region disappears and is said to be pinched-off.
- Current saturates at constant value, independent of $v_{DS.}$
- Saturation region operation mostly used for analog amplification.

NMOS Transistor:
Saturation Region (cont.)



$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2 \quad \text{for} \quad v_{DS} \geq v_{GS} - V_{TN}$$

$v_{DSAT} = v_{GS} - V_{TN}$ is termed the saturation or pinch-off voltage

Transconductance of an MOS Device

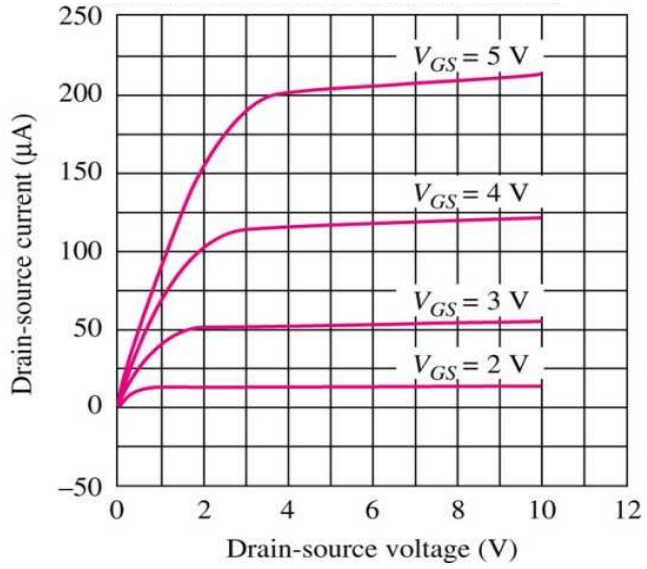
- Transconductance relates the change in drain current to a change in gate-source voltage

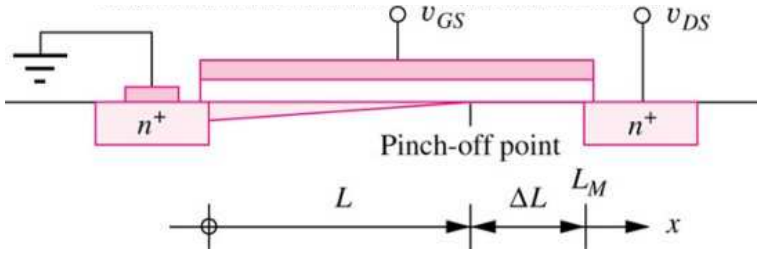
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q-pt}$$

- Taking the derivative of the expression for the drain current in saturation region,

$$g_m = K_n' \frac{W}{L}\left(V_{GS} - V_{TN}\right) = \frac{2I_D}{V_{GS} - V_{TN}}$$

Channel-Length Modulation



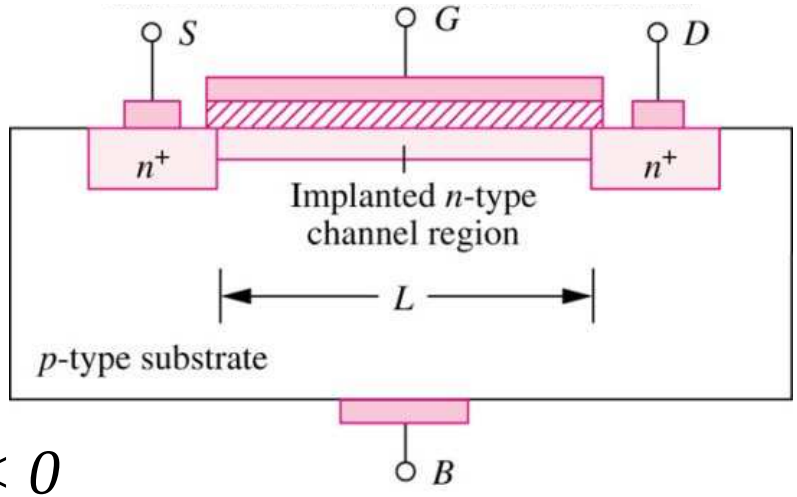


- As v_{DS} increases above v_{DSAT}, the length of the depleted channel beyond the pinch-off point, ΔL, increases and the actual L decreases.
- i_D increases slightly with v_{DS} instead of being constant.

$$i_D = \frac{K_n'}{2}\frac{W}{L}\left(v_{GS} - V_{TN}\right)^2\left(1 + \lambda v_{DS}\right)$$

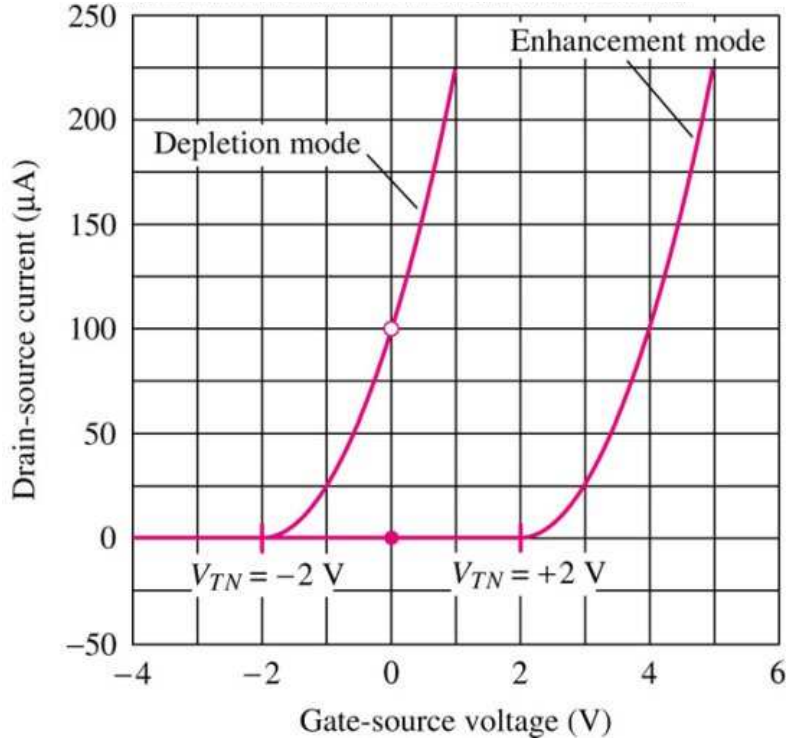
λ = channel length modulation parameter

Depletion-Mode MOSFETS



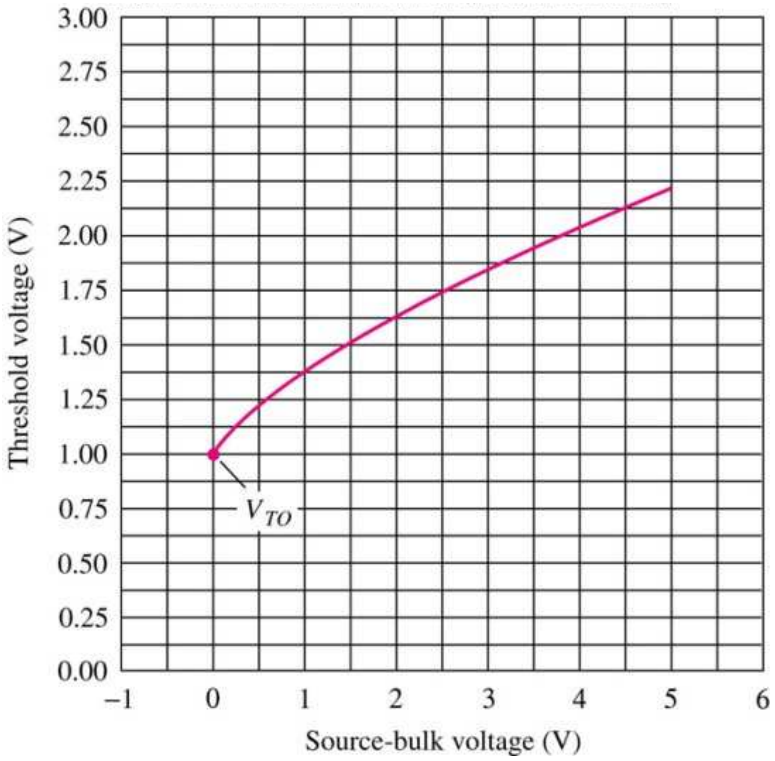
- NMOS transistors with $V_{TN} < 0$
- Ion implantation process is used to form a built-in n-type channel in the device to connect source and drain by a resistive channel
- Non-zero drain current for $v_{GS} = 0$
- Negative v_{GS} required to turn device off.

Transfer Characteristics of MOSFETS
Enhancement- & Depletion-Mode Devices



- Transfer Characteristic: Plots drain current versus gate-source voltage for a fixed drain-source voltage

Body Effect or Substrate Sensitivity



- Non-zero v_{SB} changes threshold voltage, causing substrate sensitivity modeled by

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

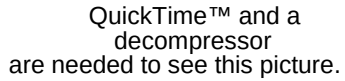
where

V_{TO} = threshold voltage for $v_{SB} = 0$

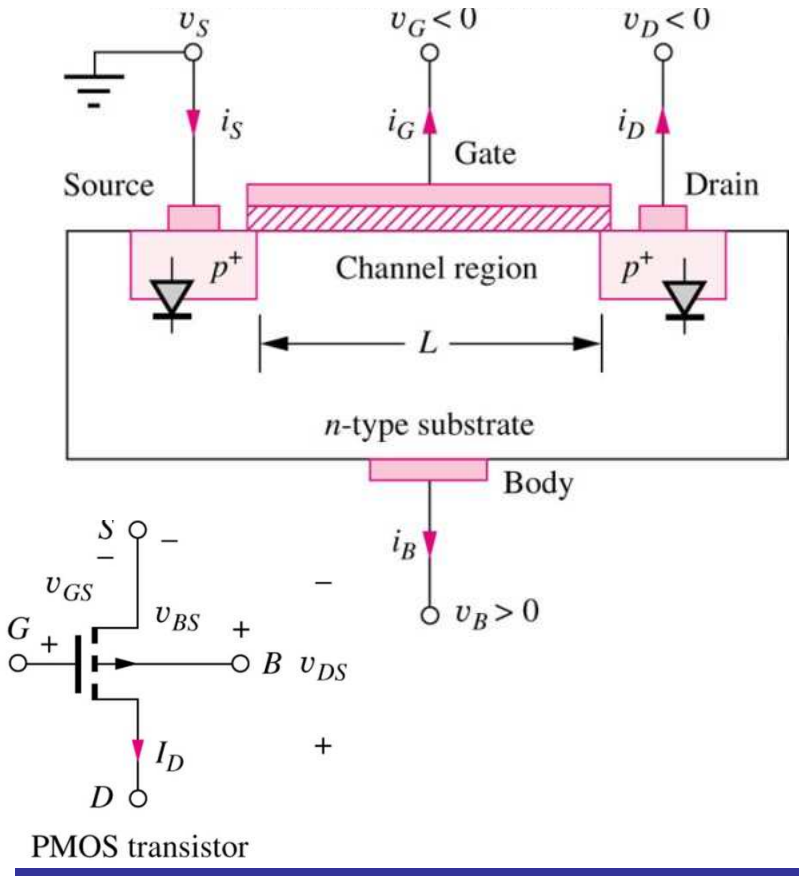
γ = body - effect parameter $\left(\sqrt{\text{V}}\right)$

$2\phi_F$ = surface potential (V)

NMOS Model Summary

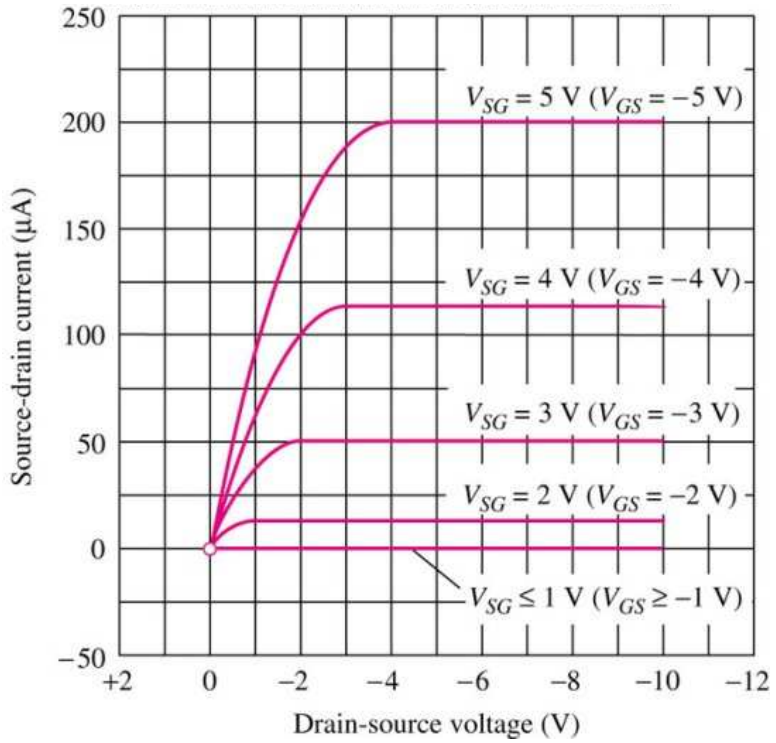


PMOS Transistors:
Enhancement-Mode Structure



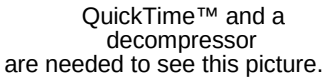
- p-type source and drain regions in an n-type substrate.
- $v_{GS} < 0$ required to create p-type inversion layer in channel region
- For current flow, $v_{GS} < V_{TP}$
- To maintain reverse bias on source-substrate and drain-substrate junctions, $v_{SB} < 0$ and $v_{DB} < 0$
- Positive bulk-source potential causes V_{TP} to become more negative

PMOS Transistors:
Output Characteristics

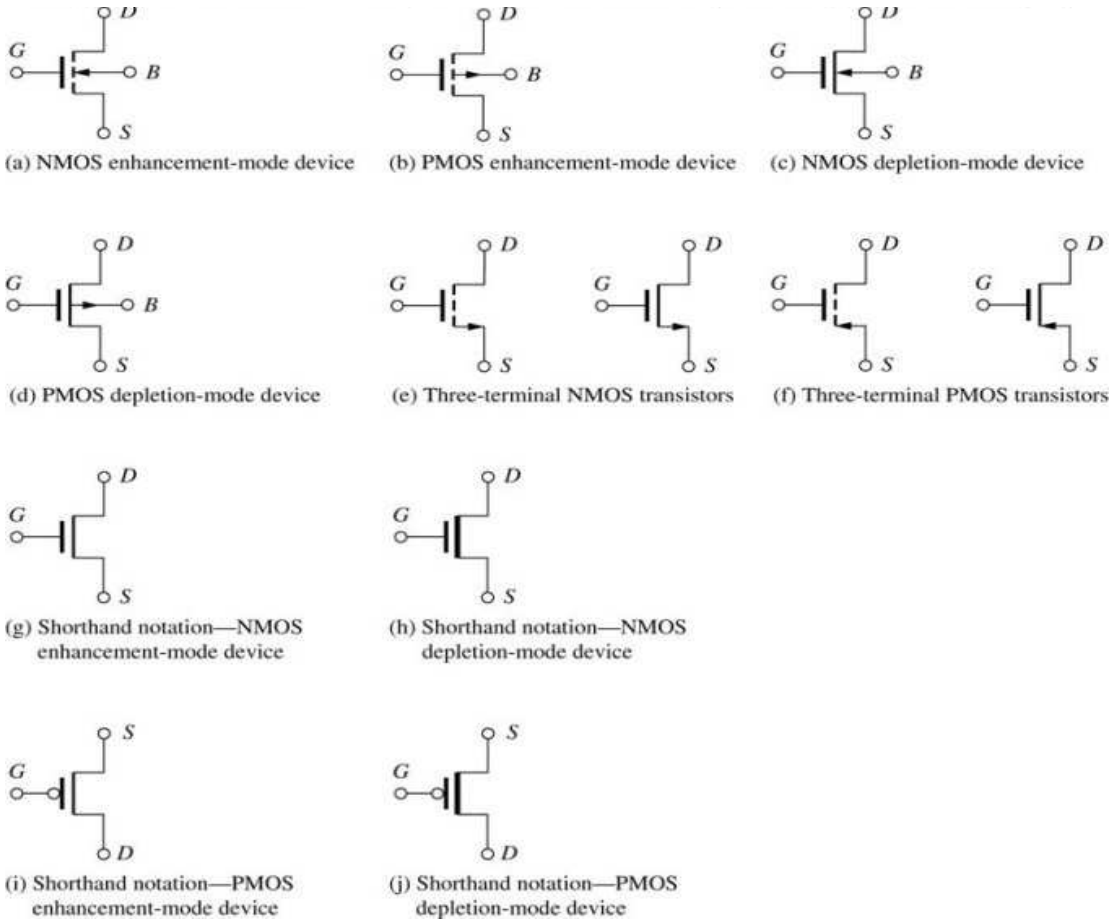


- For $v_{GS} > V_{TP}$, transistor is off.
- For more negative v_{GS}, drain current increases in magnitude.
- PMOS device is in the triode region for small values of V_{DS} and in saturation for larger values.
- Remember $V_{TP} < 0$ for an enhancement mode transistor

PMOS Model Summary



MOSFET Circuit Symbols

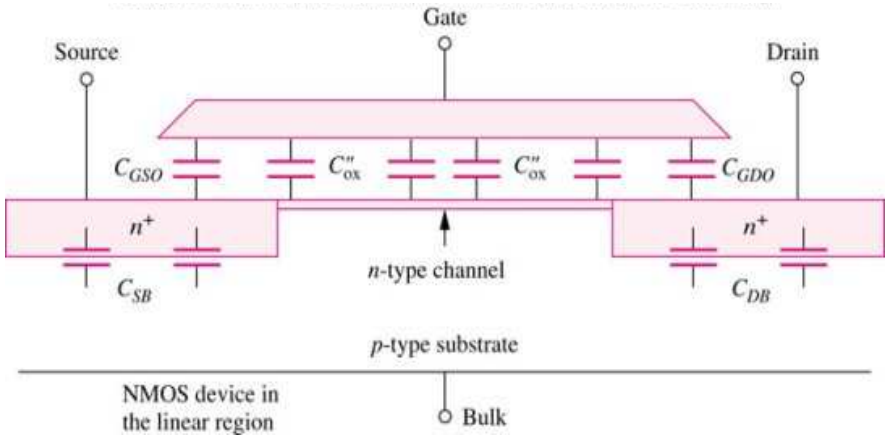


- (g) and(i) are the most commonly used symbols in VLSI logic design.
- MOS devices are symmetric.
- In NMOS, n^+ region at higher voltage is the drain.
- In PMOS p^+ region at lower voltage is the drain

Internal Capacitances in Electronic Devices

- Limit high-frequency performance of the electronic device they are associated with.
- Limit switching speed of circuits in logic applications
- Limit frequency at which useful amplification can be obtained in amplifiers.
- MOSFET capacitances depend on region of operation and are non-linear functions of voltages at device terminals.

NMOS Transistor Capacitances:
Triode Region



$$C_{GS} = \frac{C_{GC}}{2} + C_{GSO}W = C''_{ox}\frac{WL}{2} + C_{GSO}W$$

$$C_{GD} = \frac{C_{GC}}{2} + C_{GDO}W = C''_{ox}\frac{WL}{2} + C_{GDO}W$$

C''_{ox} = Gate-channel capacitance per unit area(F/m^2).

C_{GC} = Total gate channel capacitance.

C_{GS} = Gate-source capacitance.

C_{GD} = Gate-drain capacitance.

C_{GSO} and C_{GDO} = overlap capacitances (F/m).

NMOS Transistor Capacitances:
Triode Region (cont.)

$$C_{SB} = C_J A_S + C_{JSW} P_S$$

$$C_{DB} = C_J A_D + C_{JSW} P_D$$

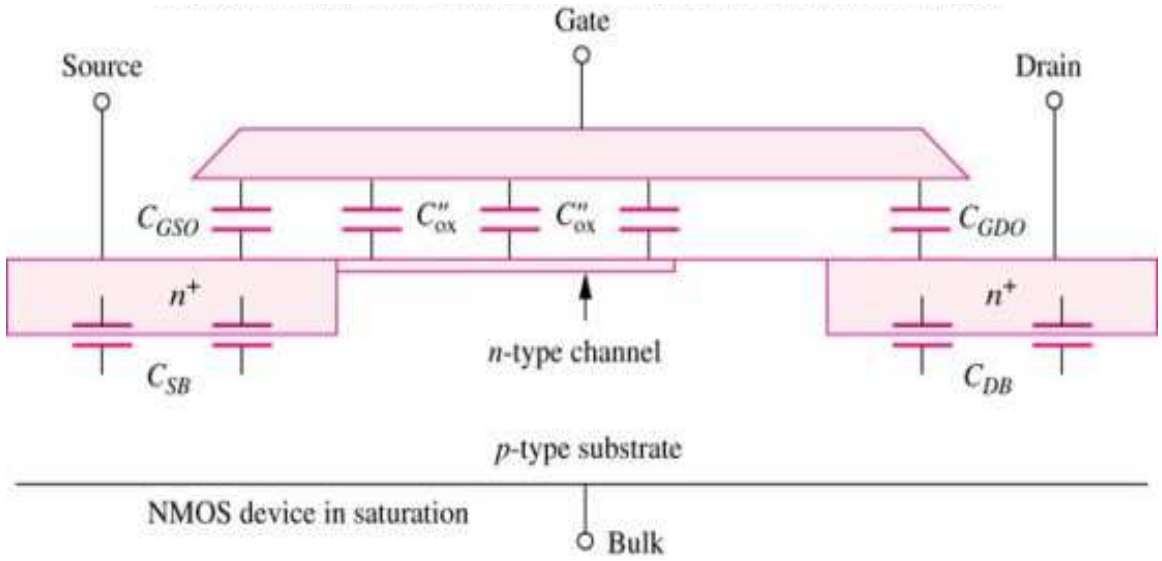
C_{SB} = Source-bulk capacitance.

C_{DB} = Drain-bulk capacitance.

A_S and A_D = Junction bottom area capacitance of the source and drain regions.

P_S and P_D = Perimeter of the source and drain junction regions.

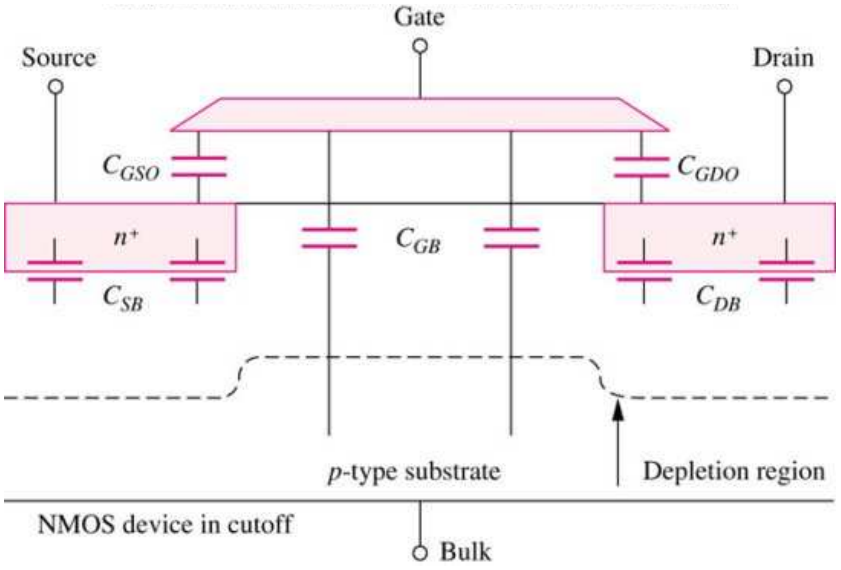
NMOS Transistor Capacitances:
Saturation Region



- Drain no longer connected to channel

$$C_{GS} = \frac{2}{3} C_{GC} + C_{GSO} W \qquad C_{GD} = \frac{2}{3} C_{GDO} W$$

NMOS Transistor Capacitances:
Cutoff Region



- Conducting channel region completely gone.

C_{GB} = gate-bulk capacitance

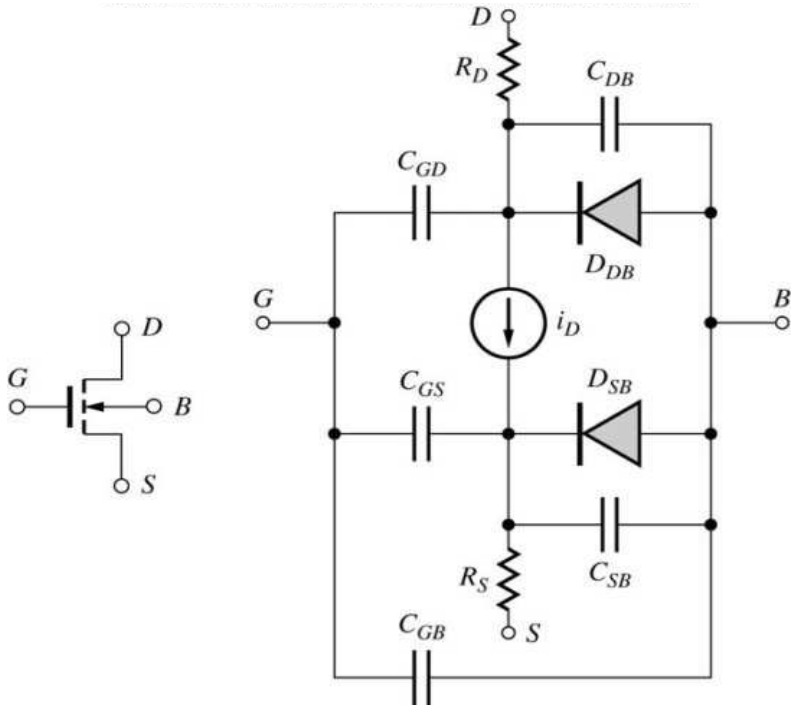
C_{GBO} = gate-bulk capacitance per unit width.

$$C_{GS} = C_{GSO}W$$

$$C_{GD} = C_{GDO}W$$

$$C_{GB} = C_{GBO}W$$

SPICE Model for NMOS Transistor



Typical default values used by SPICE:

KP = 50 or 20 μA/V^2

$\gamma = 0$

$\lambda = 0$

V_{TO} = 1 V

μ_n or μ_p = 500 or 200 cm^2/V-s

$2\Phi_F$ = 0.6 V

$C_{GDO} = C_{GSO} = C_{GBO} = C_{JSW} = 0$

T_{ox} = 100 nm

MOS Transistor Scaling
Scale Factor α

- Drain current:

$$K_n^* = \mu_n \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} = \alpha \mu_n \frac{\varepsilon_{ox}}{T_{ox}} \frac{W}{L} = \alpha K_n$$

$$i_D^* = \mu_n \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} \left(\frac{v_{GS}}{\alpha} - \frac{V_{TN}}{\alpha} - \frac{v_{DS}}{2\alpha} \right) \frac{v_{DS}}{2\alpha} = \frac{i_D}{\alpha}$$

- Gate Capacitance:

$$C_{GC}^* = \left(C_{ox}^{''} \right)^* W^* L^* = \frac{\varepsilon_{ox}}{T_{ox}/\alpha} \frac{W/\alpha}{L/\alpha} = \frac{C_{GC}}{\alpha}$$

$$\tau^* = C_{GC}^* \frac{\Delta V^*}{i_D^*} = \frac{\tau}{\alpha}$$

where τ is the circuit delay in a logic circuit.

MOS Transistor Scaling
Scale Factor α (cont.)

- Circuit and Power Densities:

$$P^* = V_{DD}^* i_D^* = \frac{V_{DD}}{\alpha}\frac{i_D}{\alpha} = \frac{P}{\alpha^2}$$

$$\frac{P^*}{A^*} = \frac{P^*}{W^* L^*} = \frac{P/\alpha^2}{(W/\alpha)(L/\alpha)} = \frac{P}{A}$$

extremely important result!

- Power-Delay Product:

$$PDP^* = P^*\tau^* = \frac{P}{\alpha^2}\frac{\tau}{\alpha} = \frac{PDP}{\alpha^3}$$

- Cutoff Frequency:

$$\omega_T = \frac{g_m}{C_{GC}} = \frac{\mu_n}{L^2}\left(V_{GS} - V_{TN}\right)$$

f_T improves with square of channel length reduction

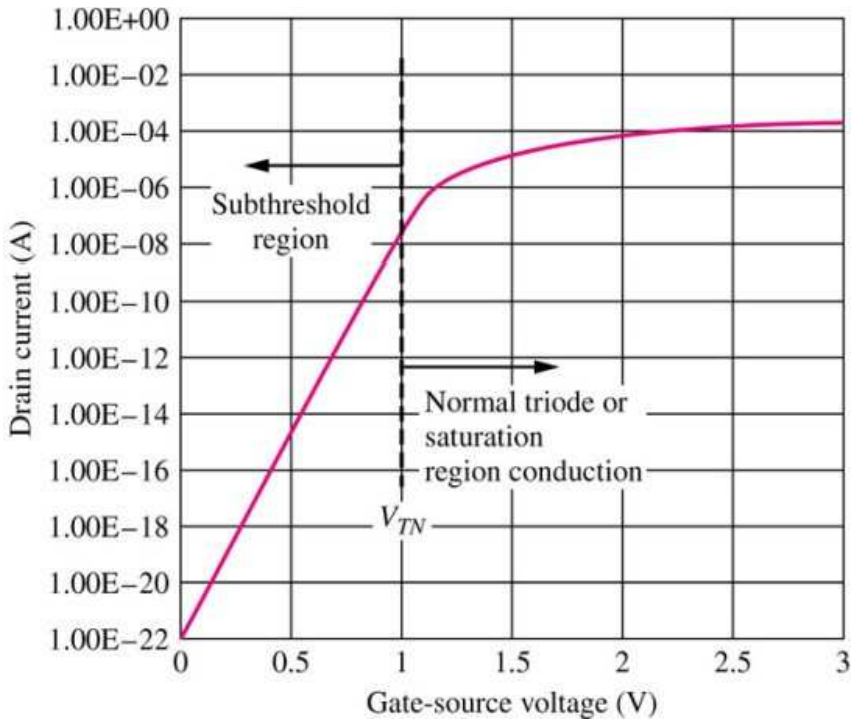
MOS Transistor Scaling (cont.)

- High Field Limitations:
  - High electric fields arise if technology is scaled down with supply voltage constant.
  - Causes reduction in mobility of MOS transistor, breakdown of linear relationship between mobility and electric field and carrier velocity saturation.
  - Ultimately results in reduced long-term reliability and breakdown of gate oxide or *pn* junction.
  - Drain current in saturation region is linearized to

$$i_D = \frac{C_{ox}^{"} W}{2}\left(v_{GS} - V_{TN}\right)v_{SAT}$$

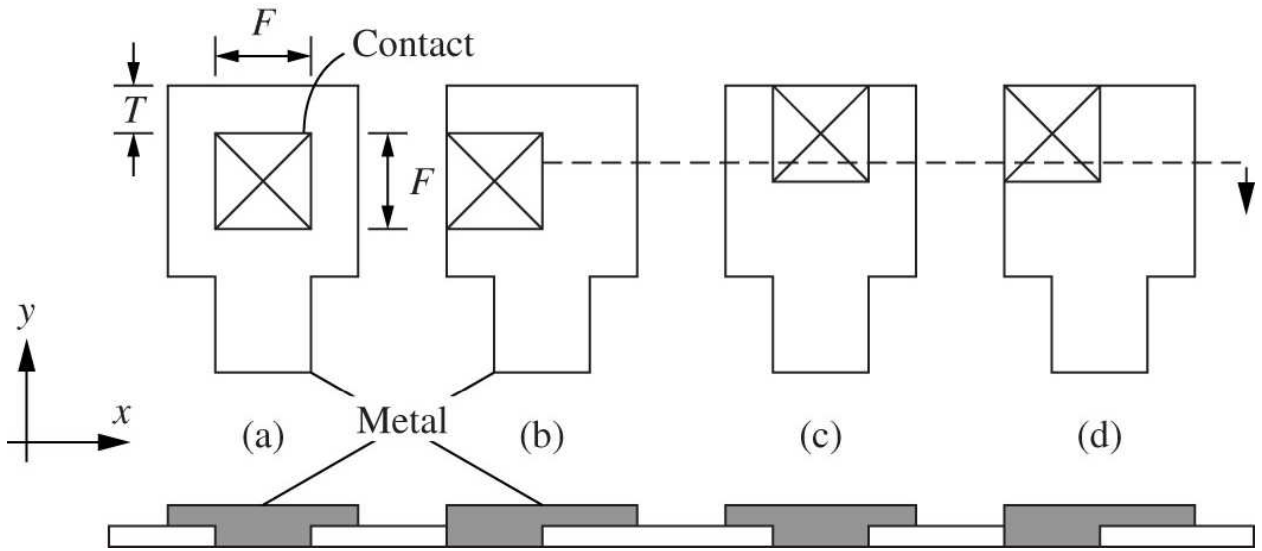
where v_{SAT} is carrier saturation velocity

MOS Transistor Scaling (cont.)



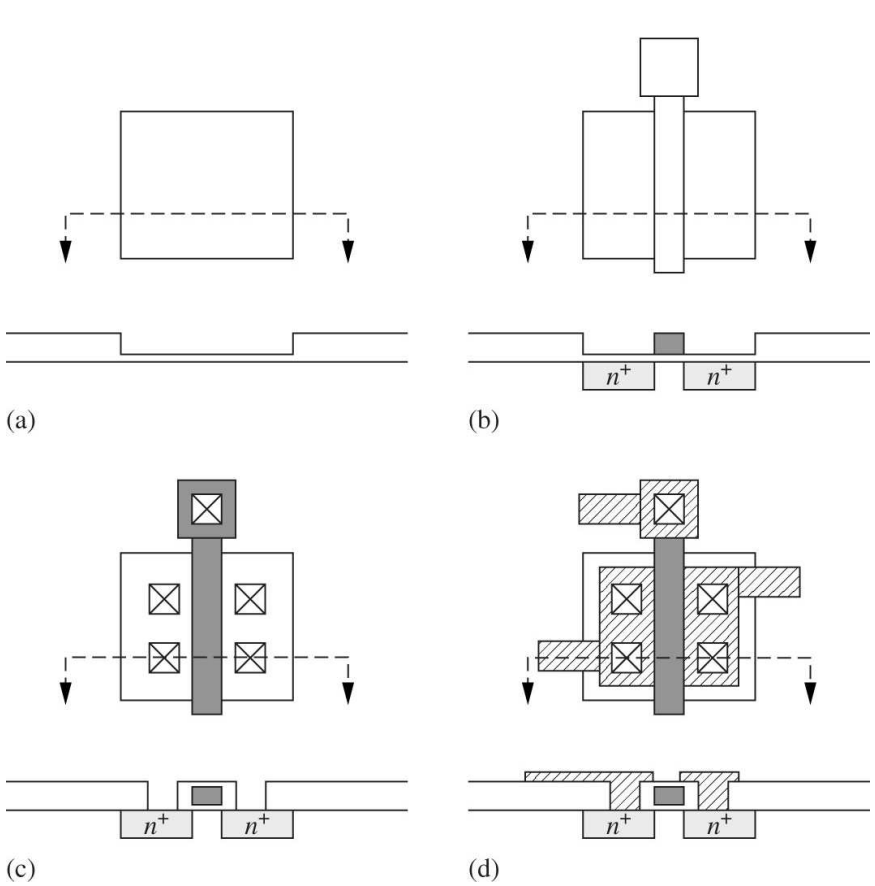
- Sub-threshold Conduction:
  - i_D decreases exponentially for $v_{GS} < V_{TN.}$
  - Reciprocal of the slope in mV/decade gives the turn-off rate for the MOSFET.
  - V_{TN} should be reduced if dimensions are scaled down. However, curve in sub-threshold region shifts horizontally instead of scaling with V_{TN}

Process-defining Factors



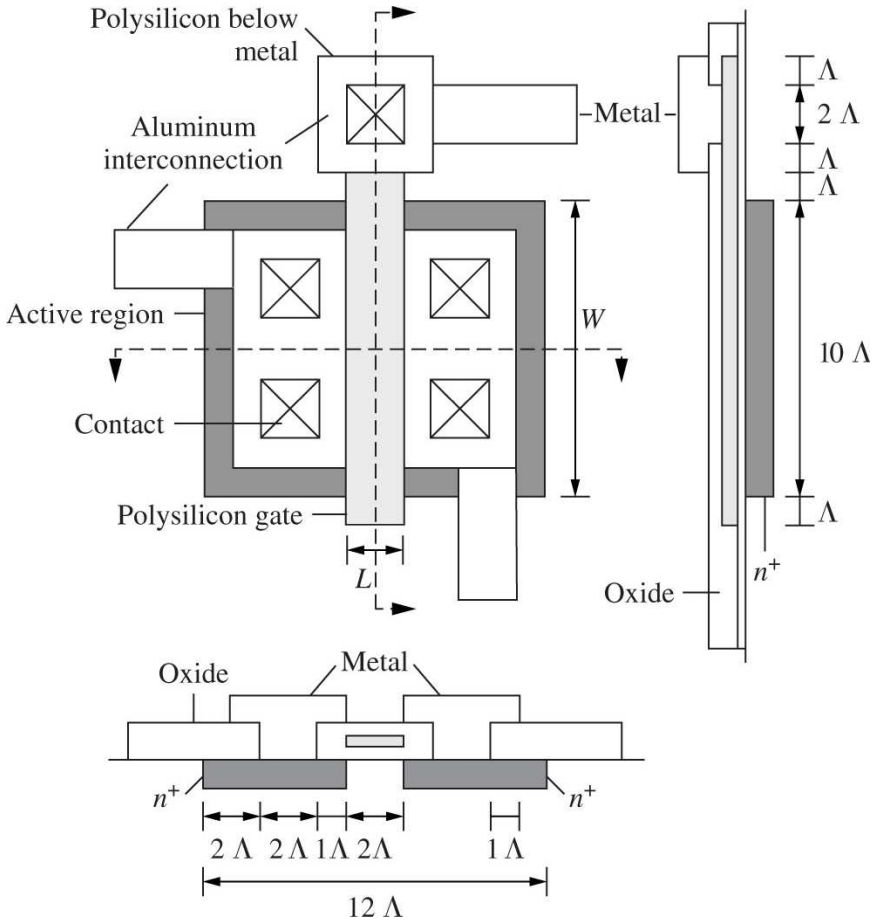
- **Minimum Feature Size** F : Width of smallest line or space that can be reliably transferred to the wafer surface using a given generation of lithographic manufacturing tools
- **Alignment Tolerance** T: Maximum misalignment that can occur between two mask levels during fabrication

Mask Sequence
Polysilicon-Gate Transistor



- Mask 1: Defines active area or thin oxide region of transistor
- Mask 2: Defines polysilicon gate of transistor, aligns to mask 1
- Mask 3: Delineates the contact window, aligns to mask 2.
- Mask 4: Delineates the metal pattern, aligns to mask 3.
- Channel region of transistor formed by intersection of first two mask layers. Source and Drain regions formed wherever mask 1 is not covered by mask 2

Basic Ground Rules for Layout



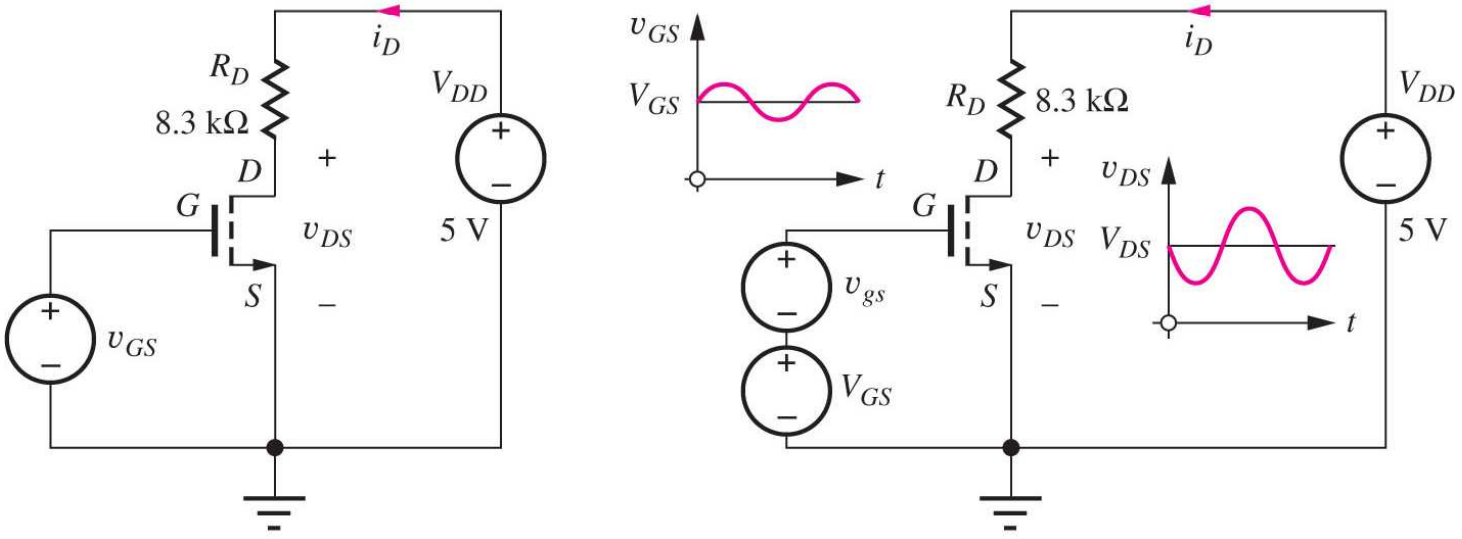
- F = 2 Λ
- T = F/2 = Λ

  Λ could be 1, 0.5, 0.25 μm, etc.

- W/L = 10Λ/2Λ = 5/1
- Transistor Area = 120 Λ^2

MOSFET Biasing

- 'Bias' sets the dc operating point around which the device operates.
- The 'signal' is actually comprised of relatively small changes in the voltages and/or currents.
- Remember (Total = dc + signal): $v_{GS} = V_{GS} + v_{gs}$ and $i_D = I_D + id$



Bias Analysis Approach

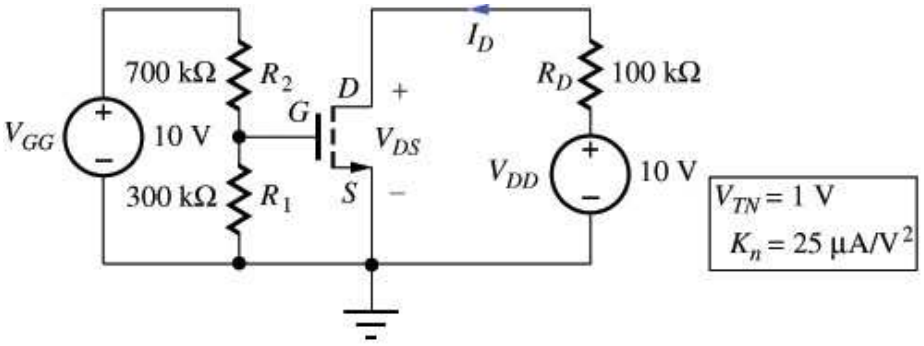
- Assume an operation region (generally the saturation region)
- Use circuit analysis to find V_{GS}
- Use V_{GS} to calculate I_D, and I_D to find V_{DS}
- Check validity of operation region assumptions
- Change assumptions and analyze again if required.

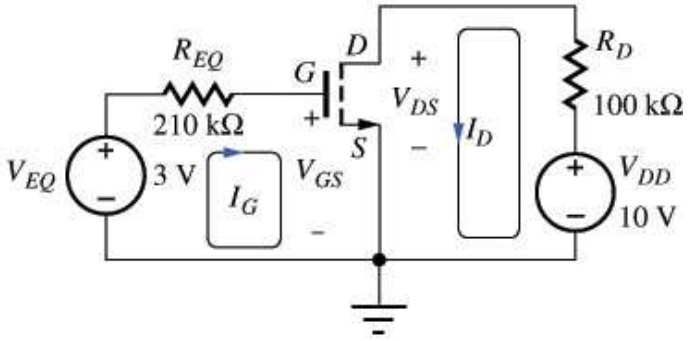
NOTE: An enhancement-mode device with $V_{DS} = V_{GS}$ is always in saturation

Four-Resistor and Two-Resistor Biasing

- Provide excellent bias for transistors in discrete circuits.
- Stabilize bias point with respect to device parameter and temperature variations using negative feedback.
- Use single voltage source to supply both gate-bias voltage and drain current.
- Generally used to bias transistors in saturation region.
- Two-resistor biasing uses fewer components that four-resistor biasing

Bias Analysis - Example 1:
Constant Gate-Source Voltage Biasing





Problem: Find Q-pt (I_D, V_{DS} , V_{GS})

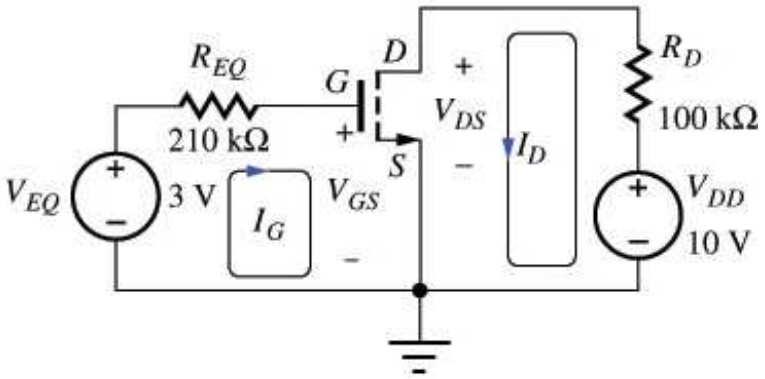
Approach: Assume operating region, find Q-point, check to see if result is consistent with assumed region of operation

Assumption: Transistor is saturated, $I_G = I_B = 0$

Analysis: Simplify circuit with Thévenin transformation to find V_{EQ} and R_{EQ} for gate-bias voltage. Find V_{GS} and then use this to find I_D. With I_D, we can then calculate V_{DS}.

Bias Analysis - Example 1:

Constant Gate-Source Voltage Biasing (cont.)



Since $I_G = 0$,

$$V_{EQ} = I_G R_{EQ} + V_{GS} = V_{GS}$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2$$

$$I_D = \frac{25x10^{-6}}{2}\frac{A}{V^2}(3-1)^2 V^2 = 50.0\ \mu A$$

$$V_{DD} = I_D R_D + V_{DS}$$

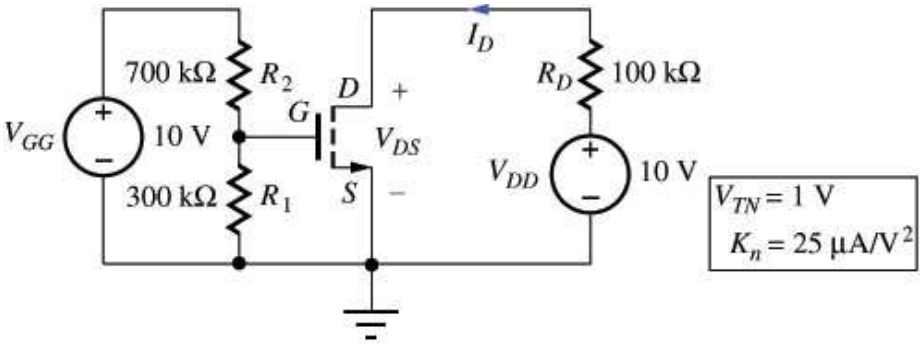
$$V_{DS} = 10V - (50\mu A)(100K) = 5.00\ V$$

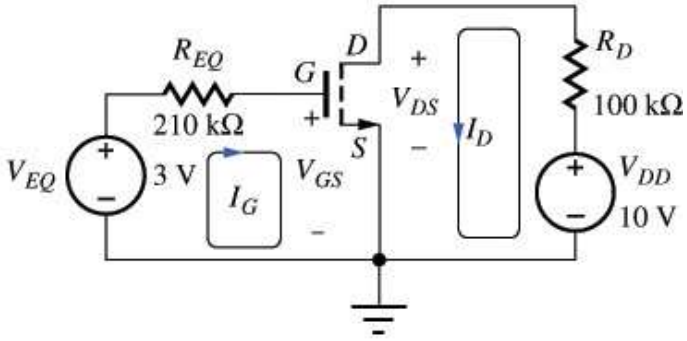
Check: $V_{DS} > V_{GS}$-V_{TN}. Hence saturation region assumption is correct.

Q-pt: (50.0 μA, 5.00 V) with V_{GS}= 3.00 V

Discussion: The Q-point of this circuit is quite sensitive to changes in transistor characteristics, so it is not widely used.

Bias Analysis - Example 2:
Load Line Analysis





Problem: Find Q-pt (I_D, V_{DS} , V_{GS})

Approach: Find an equation for the load line. Use this to find Q-pt at intersection of load line with device characteristic.

$$V_{DD} = I_D R_D + V_{DS}$$

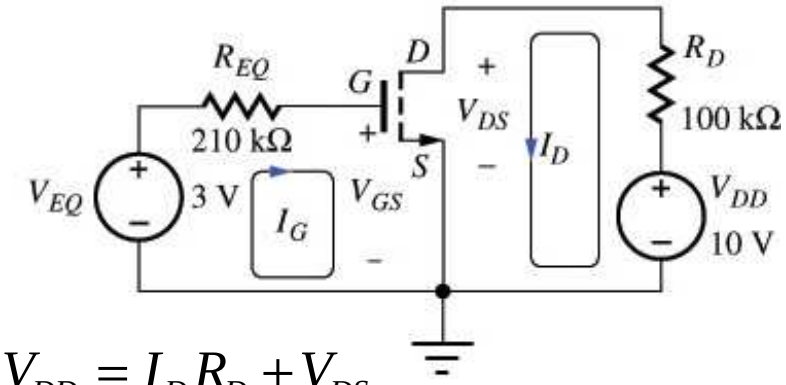
Assumption: Transistor is saturated, $I_G = I_B = 0$

Analysis: For circuit values above, load line becomes

$$10V = I_D(100K) + V_{DS}$$

Use this to find two points on the load line.

Bias Analysis - Example 2:
Load Line Analysis (cont.)



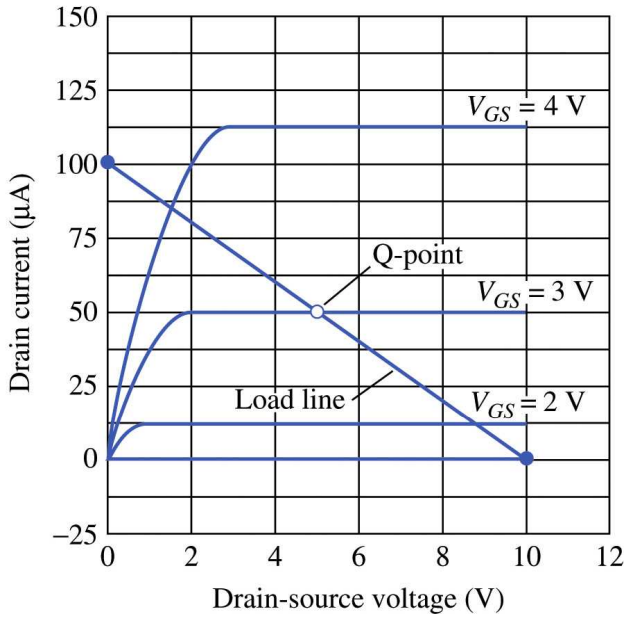
$$V_{DD} = I_D R_D + V_{DS}$$

$$10 = 10^5 I_D + V_{DS}$$

For $V_{DS} = 0$, $I_D = 100$ uA

For $I_D = 0$, $V_{DS} = 10$ V

Plotting the line on the transistor output characteristic yields Q-pt at intersection with $V_{GS} = 3$V device curve.

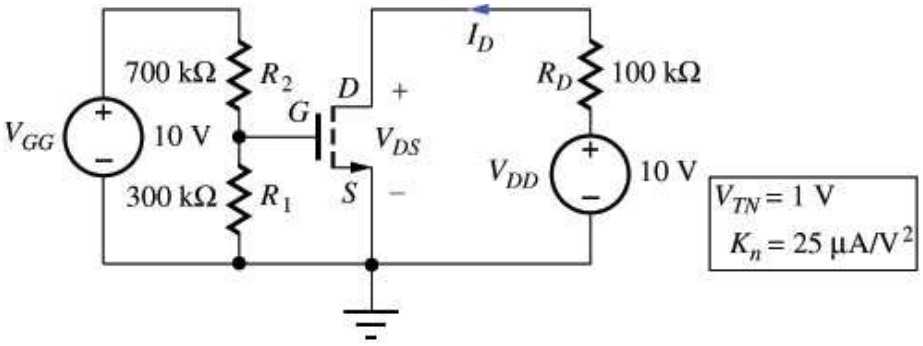


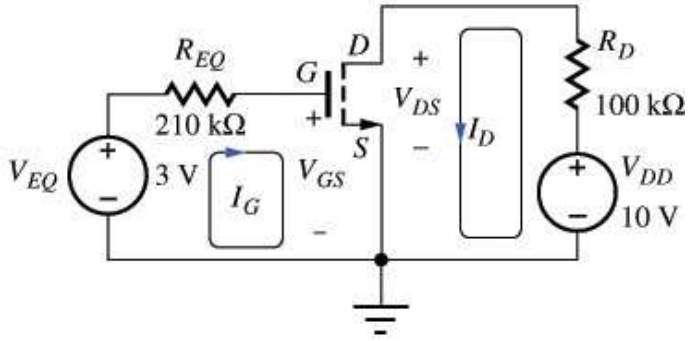
Check: The load line approach agrees with previous calculation.

Q-pt: (50.0 μA, 5.00 V) with V_{GS} = 3.00 V

Discussion: Q-pt is clearly in the saturation region. Graphical load line is good visual aid to see device operating region.

Bias Analysis - Example 3:
Constant Gate-Source Voltage Biasing with Channel-Length Modulation





Problem: Find Q-pt (I_D, V_{DS}, V_{GS}) of previous example, given $\lambda = 0.02$ V^{-1}.

Approach: Assume operation region, find Q-point, check to see if result is consistent with operation region

Assumption: Transistor is saturated, $I_G = I_B = 0$

Analysis: Simplify circuit with Thévenin transformation to find V_{EQ} and R_{EQ} for gate-bias voltage. Find V_{GS} and then use this to find I_D. With I_D, we can then calculate V_{DS}.

Bias Analysis - Example 3:
Constant Gate-Source Voltage Biasing with Channel-Length Modulation (cont.)

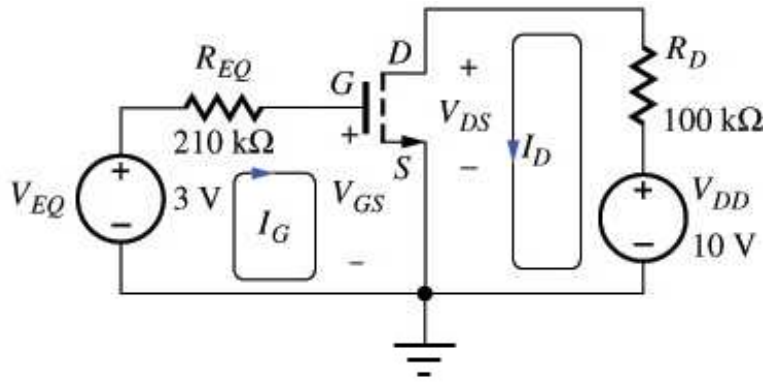
$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2\left(1+\lambda V_{DS}\right)$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 10 - \frac{25x10^{-6}}{2}\left(10^5\right)\left(3-1\right)^2\left(1+0.02V_{DS}\right)$$

$$V_{DS} = 4.55\ V$$

$$I_D = \frac{25x10^{-6}}{2}\left(3-1\right)^2\left[1+0.02\left(4.55\right)\right] = 54.5\ \mu A$$

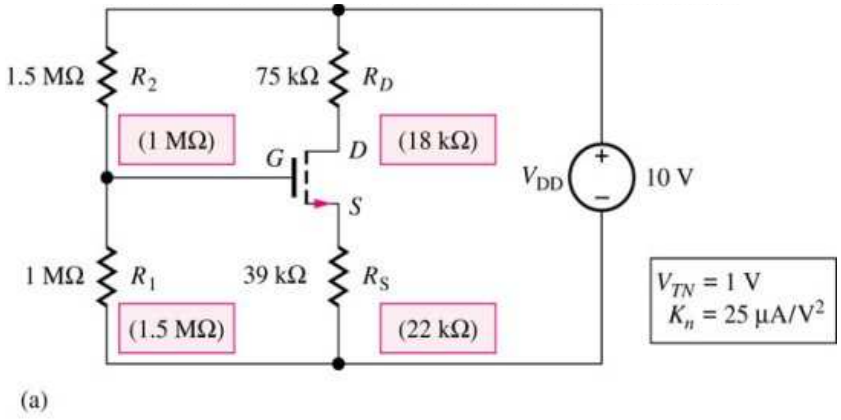


Check: $V_{DS} > V_{GS} - V_{TN}$. Hence the saturation region assumption is correct.

Q-pt: (54.5 μA, 4.55 V) with V_{GS} = 3.00 V

Discussion: The bias levels have changed by about 10% (54.5 μA vs 50 μA). Typically, component values will vary more than this, so there is little value in including λ effects in most circuits.

Bias Analysis - Example 4:
Four-Resistor Biasing



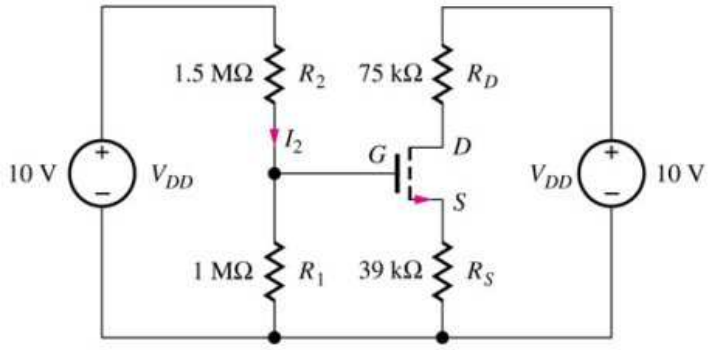
(a)

Assumption: Transistor is saturated, $I_G = I_B = 0$

Analysis: First, simplify circuit, split V_{DD} into two equal-valued sources and apply Thévenin transformation to find V_{EQ} and R_{EQ} for gate-bias voltage

Problem: Find Q-pt (I_D, V_{DS})

Approach: Assume operation region, find Q-point, check to see if result is consistent with operation region

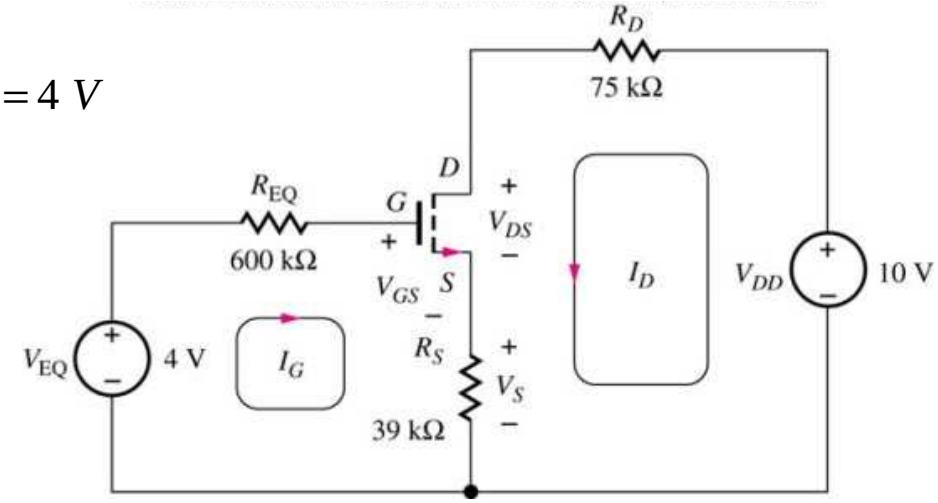


(b)

Bias Analysis - Example 4:
Four-Resistor Biasing (cont.)

$$V_{EQ} = V_{DD}\frac{R_1}{R_1 + R_1} = 10V\frac{1M\Omega}{1M\Omega + 1.5M\Omega} = 4\ V$$

$$R_{EQ} = R_1 \| R_1 = 1M\Omega \| 1.5M\Omega = 600\ k\Omega$$



Since $I_G = 0, \quad V_{EQ} = V_{GS} + I_D R_S$

$$V_{EQ} = V_{GS} + \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 R_S$$

$$4 = V_{GS} + \frac{25x10^{-6}}{2}\left(39x10^3\right)\left(V_{GS} - 1\right)^2$$

$$V_{GS} = -2.71\ V \text{ or } +2.66\ V$$

Since $V_{GS} < V_{TN}$ for $V_{GS} = -2.71\ V$, the MOSFET would be off.

$$\therefore V_{GS} = +2.66\ V \text{ and } I_D = 34.4\ \mu\text{A}$$

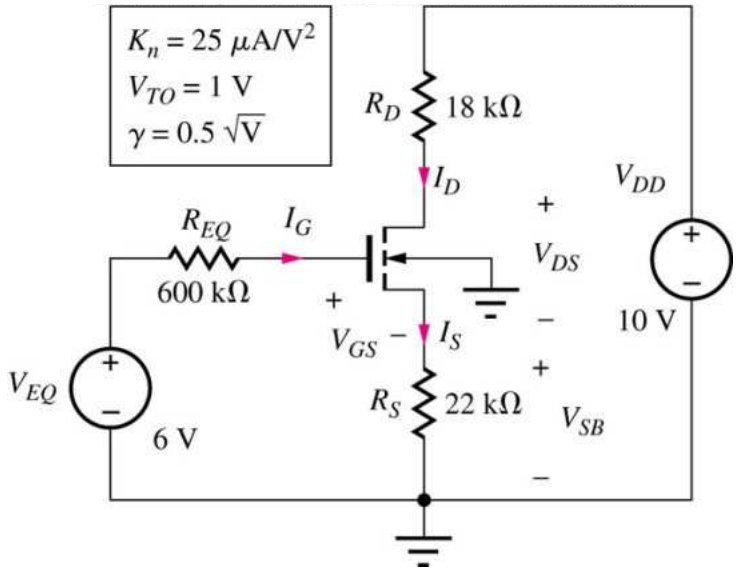
$$V_{DS} = V_{DD} - I_D R_D = 6.08\ V$$

$V_{DS} > V_{GS}$-V_{TN}. Hence the saturation region assumption is correct.

Q-pt: (34.4 μA, 6.08 V) with V_{GS} = 2.66 V

Bias Analysis - Example 5:
Four-Resistor Biasing with Body Effect

Analysis with body effect using the same assumptions as in example 1:



$$V_{GS} = V_{EQ} - I_D R_S = 6 - 22000 I_D$$

$$V_{SB} = I_D R_S = +22000 I_D$$

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

$$V_{TN} = 1 + 0.5\left(\sqrt{v_{SB} + 0.6} - \sqrt{0.6}\right)$$

$$I_D' = \frac{25x10^{-6}}{2}\left(V_{GS} - V_{TN}\right)^2$$

Iterative solution can be found using the following steps:

- Estimate value of I_D and use it to find V_{GS} and V_{SB}
- Use V_{SB} to calculate V_{TN}
- Find I_D' using above 2 steps
- If I_D' is not same as original I_D estimate, start again.

Bias Analysis - Example 5:
Four-Resistor Biasing (cont.)

The iteration sequence leads to $I_D = 88.0\ \mu A$, $V_{TN} = 1.41\ V$,

$$V_{DS} = V_{DD} - I_D\left(R_D + R_S\right) = 10 - 4x10^4 I_D = 6.48\ V$$

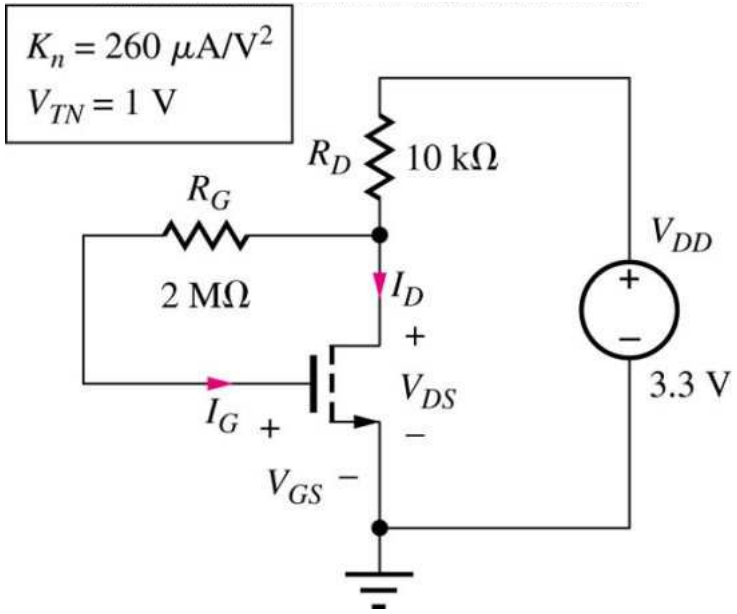
$V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.

Q-pt: (88.0 μA, 6.48 V)

Check: $V_{DS} > V_{GS} - V_{TN}$, therefore still in active region.

Discussion: Body effect has decreased current by 12% and increased threshold voltage by 40%.

Bias Analysis - Example 6:
Two-Resistor Feedback Biasing



Assumption: $I_G = I_B = 0$, transistor is saturated (since $V_{DS} = V_{GS}$)

Analysis: $V_{DS} = V_{DD} - I_D R_D$

$$V_{GS} = V_{DD} - \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 R_D$$

$$V_{GS} = 3.3 - \frac{2.6x10^{-4}}{2}\left(10^4\right)\left(V_{GS} - 1\right)^2$$

$$V_{GS} = -0.769\ V \text{ or } +2.00\ V$$

Since $V_{GS} < V_{TN}$ for V_{GS} = -0.769 V, the MOSFET would be cut-off,

$$\therefore V_{GS} = +2.00\ \text{V} \text{ and } I_D = 130\ \mu A$$

$V_{DS} > V_{GS} - V_{TN}$. Hence saturation region assumption is correct.

Q-pt: (130 μA, 2.00 V)

Bias Analysis - Example 7:
Biasing in Triode Region

Assumption: Assume saturation

Analysis: $V_{GS} = V_{DD} = 4$ V

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 = \frac{2.5x10^{-4}}{2}\left(4-1\right)^2$$

$$I_D = 1.13\ mA$$

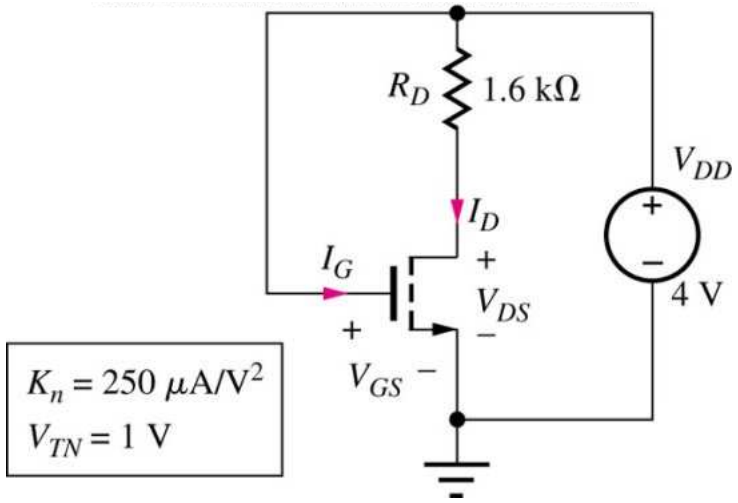
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 4 - \left(1.13x10^{-3}\right)\left(1.6x10^{3}\right) = 2.19\ V$$

But $V_{DS} < V_{GS} - V_{TN}$. Hence, saturation region operation is incorrect.

Using triode region equation:

$$I_D = K_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$$



$$4 - V_{DS} = \left(1.6x10^{3}\right)\left(2.5x10^{-4}\right)\left(4 - 1 - \frac{V_{DS}}{2}\right)V_{DS}$$

$V_{DS} = 2.30\ V$ and $I_D = 1.06\ mA$

$V_{DS} > V_{GS} - V_{TN}$, transistor is in the triode region

Q-pt:(1.06 mA, 2.3 V)

Bias Analysis - Example 8:
Two-Resistor biasing for PMOS Transistor

Assumption: $I_G = I_B = 0$; transistor is saturated

Analysis:

$$V_{GS} - I_G R_G - V_{DS} = 0 \rightarrow V_{DS} = V_{GS}$$

$$V_{DD} + V_{DS} - I_D R_D = 0$$

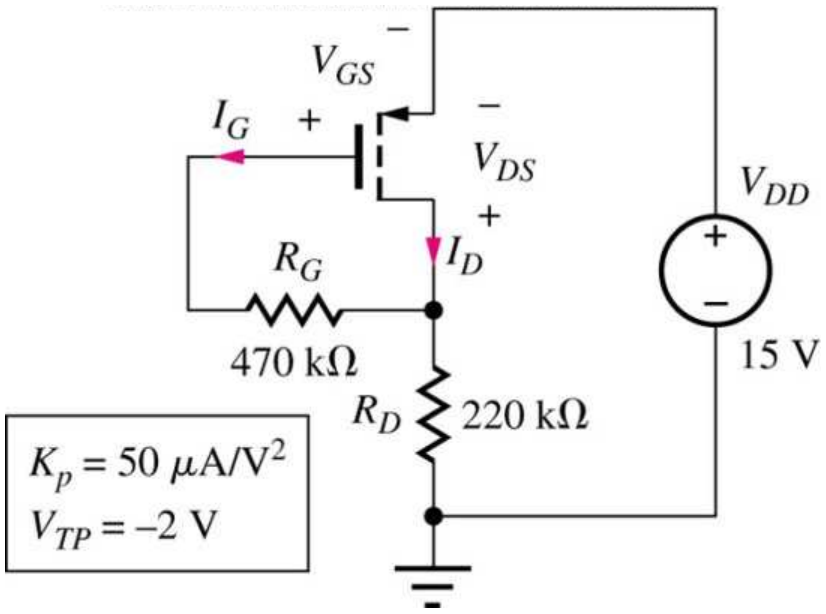
$$V_{DD} + V_{GS} - \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 R_D = 0$$

$$15 + V_{GS} - \left(2.2x10^5\right)\frac{5x10^{-5}}{2}\left(V_{GS} + 2\right)^2 = 0$$

$$V_{GS} = -0.369\ V, -3.45\ V$$

Since $V_{GS} = -0.369 > V_{TP}$, $V_{GS} = -3.45\ V$

$$I_D = 52.5\ \mu A \quad \text{and} \quad V_{DS} = -3.45\ V$$

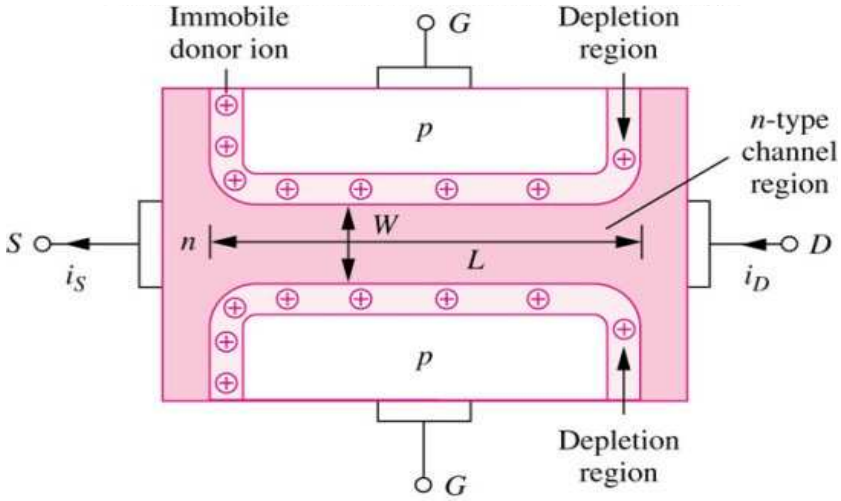


$$|V_{DS}| > |V_{GS} - V_{TP}|$$

Hence saturation assumption is correct.

Q-pt: (52.5 μA, -3.45 V)

Junction Field-Effect Transistor Structure The JFET



- *n*-type semiconductor block houses the channel region in *n*-channel JFET.
- Two *pn* junctions form the gate.
- Current enters channel at the drain and exits at source.

- Much lower input current and much higher input impedance than the BJT.
- In triode region, JFET is a voltage-controlled resistor:

$$R_{CH} = \frac{\rho}{t}\frac{L}{W}$$

ρ = resistivity of channel

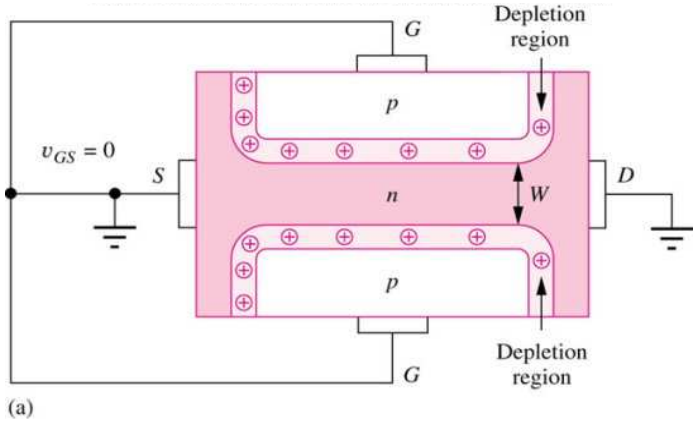
L = channel length

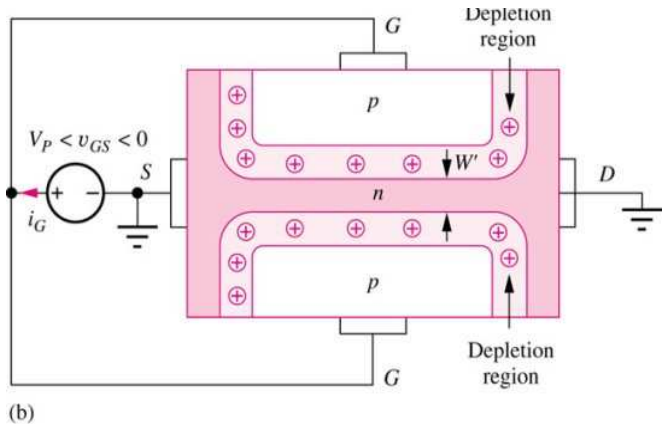
W = channel width between *pn* junction depletion regions

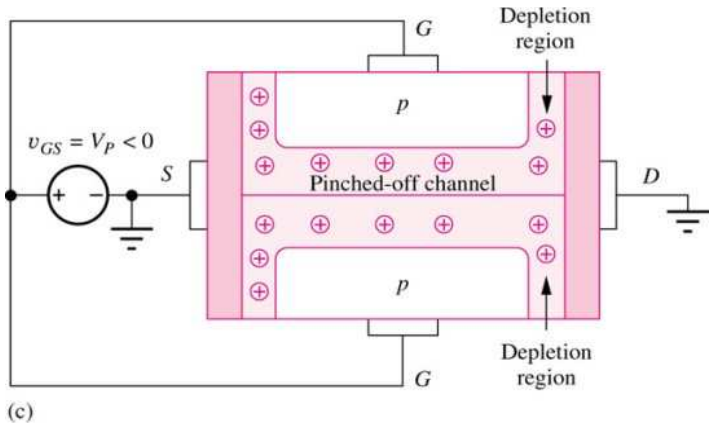
t = channel depth

- Inherently a depletion-mode device

JFET with Gate-Source Bias

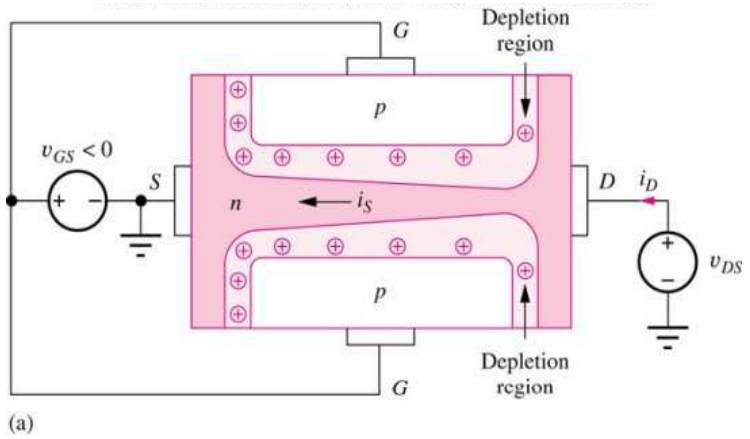




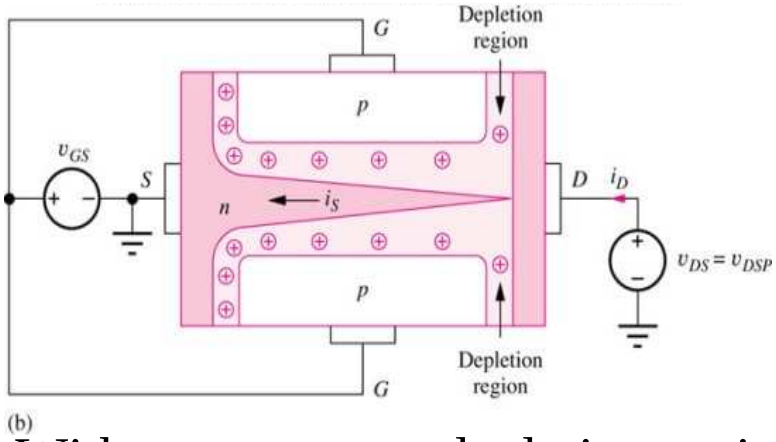


- $v_{GS} = 0$, gate isolated from channel.
- $V_P < v_{GS} < 0$, W' < W, and channel resistance increases; gate-source junction is reverse-biased, i_G almost 0.
- $v_{GS} = V_P < 0$, channel region pinched-off, channel resistance is infinite.

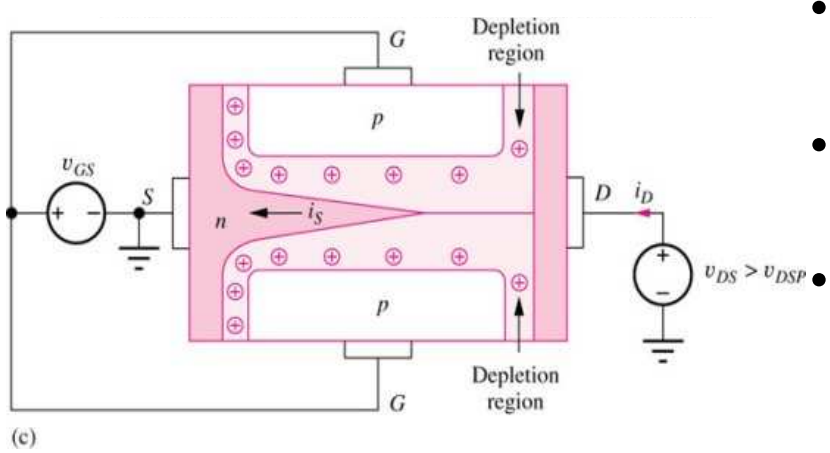
JFET Channel with Drain-Source Bias



(a)



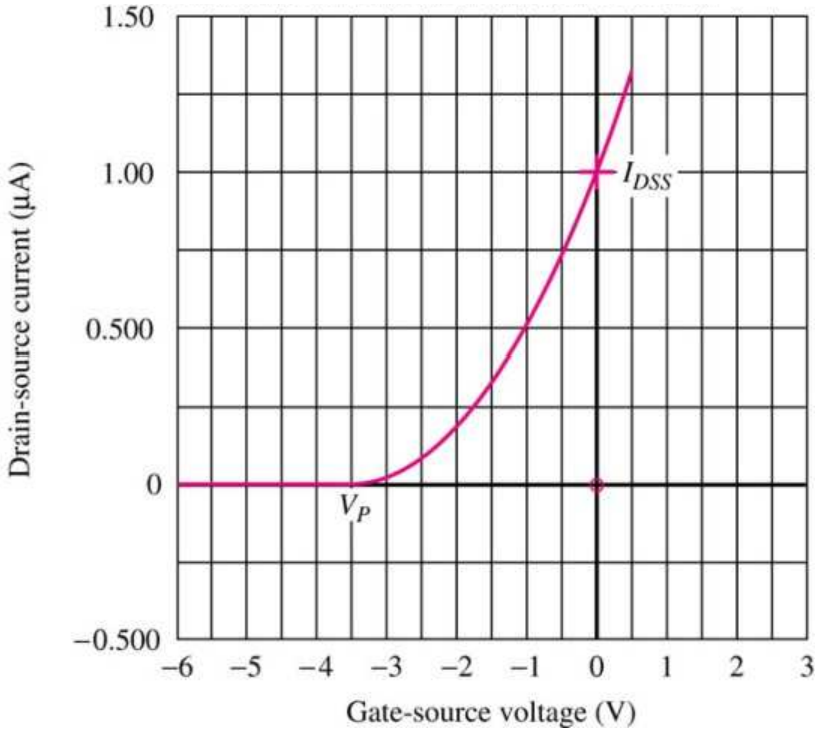
(b)



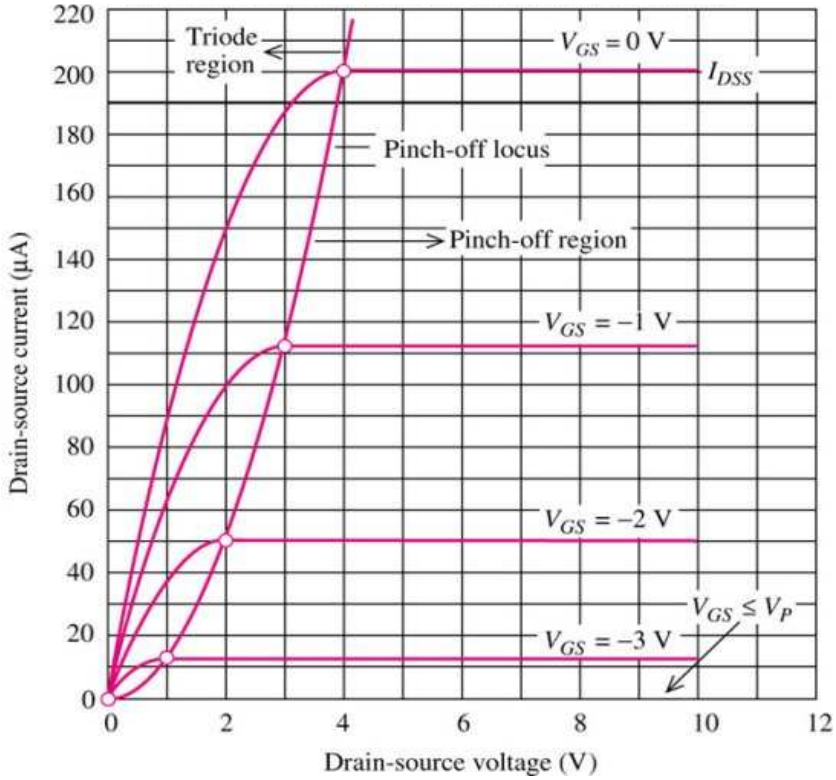
(c)

- With constant v_{GS}, depletion region near drain increases with v_{DS}.
- At $v_{DSP} = v_{GS} - V_P$, channel is totally pinched-off; i_D is saturated.
- JFET also suffers from channel-length modulation like MOSFET at larger values of v_{DS}.

n-Channel JFET
i-*v* Characteristics



Transfer Characteristics



Output Characteristics

n-Channel JFET
i-*v* Characteristics (cont.)

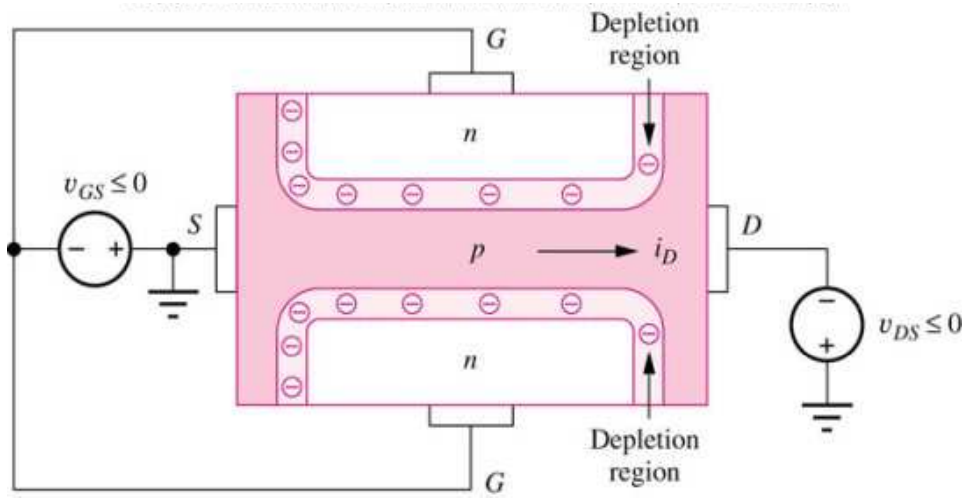
- For all regions : $i_G = 0 \quad \text{for} \quad v_{GS} \leq 0$
- In cutoff region: $i_D = 0 \quad \text{for} \quad v_{GS} \leq V_P \quad (V_P < 0)$
- In Triode region:

$$i_D = \frac{2I_{DSS}}{V_P^{\,2}}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \geq V_P \quad \text{and} \quad v_{GS} - V_P \geq V_{DS} \geq 0$$

- In pinch-off region:

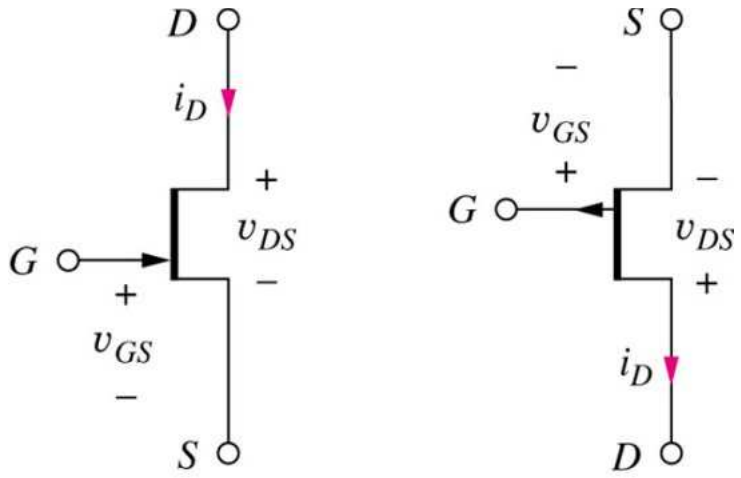
$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2\left(1 + \lambda v_{DS}\right) \quad \text{for} \quad v_{DS} \geq v_{GS} - V_P \geq 0$$

p-Channel JFET



- Polarities of *n*- and *p*-type regions of the *n*-channel JFET are reversed to get the *p*-channel JFET.
- Channel current direction and operating bias voltages are also reversed.

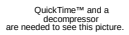
JFET Circuit Symbols



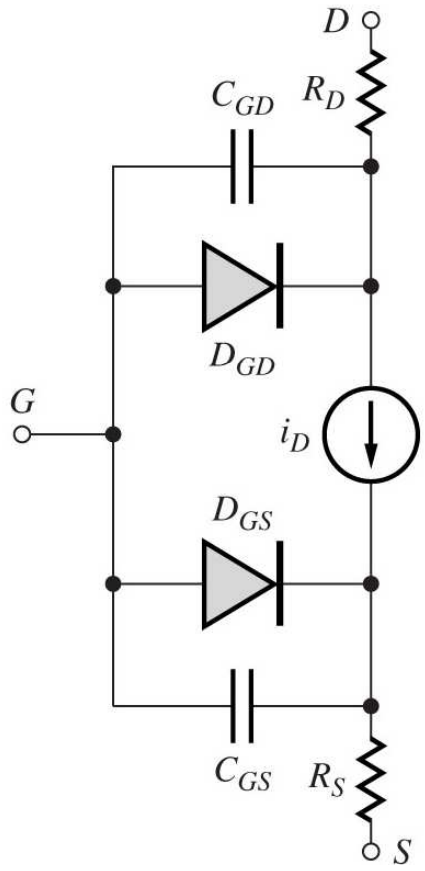
- JFET structures are symmetric like MOSFETs.
- Source and drain determined by circuit voltages.

JFET n-Channel Model Summary

JFET p-Channel Model Summary



JFET Capacitances and SPICE Modeling



C_{GD} and C_{GS} are determined by depletion-layer capacitances of reverse-biased *pn* junctions forming gate and are bias dependent.

Typical default values used by SPICE:

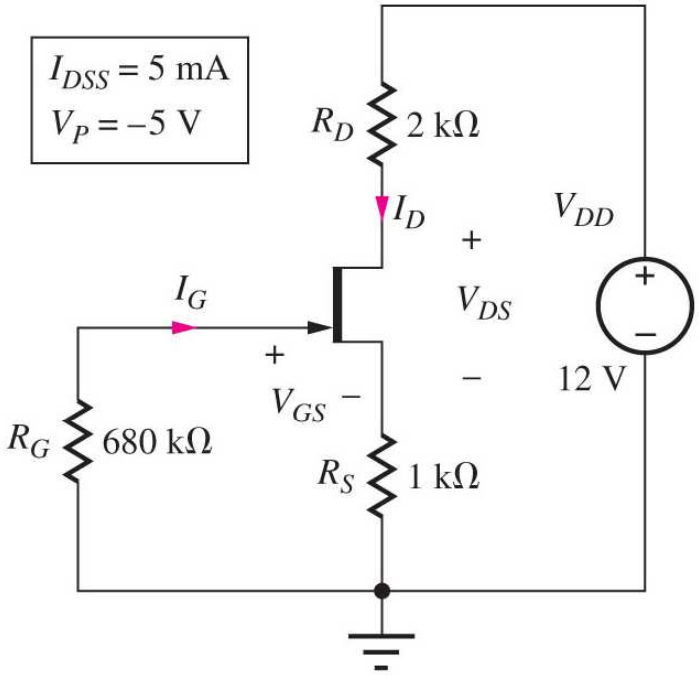
V_p = -2 V

$\lambda = C_{GD} = C_{GD} = 0$

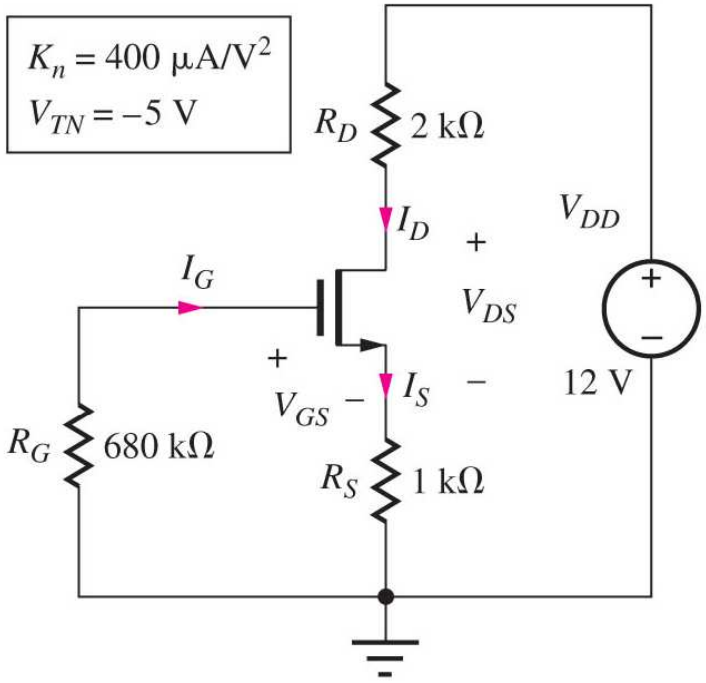
Transconductance parameter BETA

BETA = I_{DSS}/V_P^2 = 100 μA/V^2

Example:
Biasing the JFET & Depletion-Mode MOSFET



N-channel JFET



Depletion-mode MOSFET

- **Assumptions:** JFET is pinched-off, gate-channel junction is reverse-biased, reverse leakage current of gate, $I_G = 0$

Example:
Biasing JFET & Depletion-Mode MOSFET (cont.)

- **Analysis**:

Since $I_S = I_D,\ V_{GS} = -I_D R_S$

$$V_{GS} = -I_{DSS} R_S \left(1 - \frac{V_{GS}}{V_P}\right)^2 = -\left(5\times10^{-3}\,\text{A}\right)(1000\,\Omega)\left(1 - \frac{V_{GS}}{-5\text{V}}\right)^2$$

$$\therefore\ V_{GS} = -1.91\text{V},\ -13.1\text{V}$$

Since V_{GS} = -13.1 V is less than V_P = -5 V, V_{GS} = -1.91 V, and $I_D = I_S$ = 1.91 mA. Also,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) = 12 - (1.91\text{mA})(3\text{k}\Omega) = 6.27\text{V}$$

$V_{DS} > V_{GS} - V_P$. Hence pinch-off region assumption is correct and gate-source junction is reverse-biased by 1.91V.

Q-pt: (1.91 mA, 6.27 V)

End of Chapter 4